

# Compal Confidential

## Schematics Document

INTEL Auburndale BGA with IBEX core logic

Swatch UMA

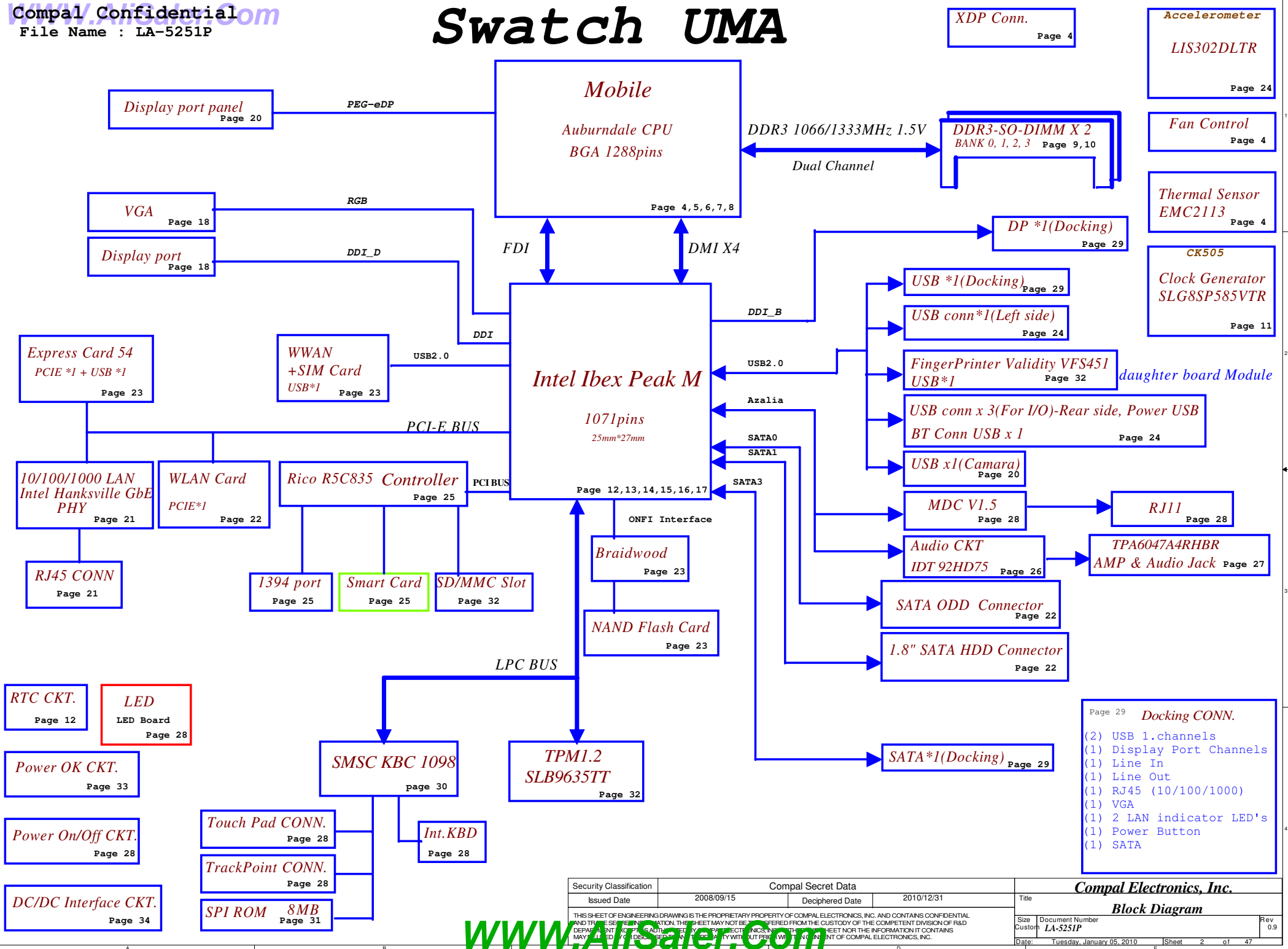
LA-5251P

2010-01-04

REV:0.9

Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b>		
Issued Date	2008/09/15	Deciphered Date	2010/12/31	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE REPRODUCED OR DISCLOSED TO ANY OTHER PERSON OR ENTITY WITHOUT THE WRITTEN PERMISSION OF COMPAL ELECTRONICS, INC.				Cover Sheet		
				Size	Document Number	Rev
				Custom	LA-5251P	0.9
Date:				Tuesday, January 05, 2010	Sheet	1 of 47

# Swatch UMA



## Voltage Rails ( O MEANS ON X MEANS OFF )

power plane State	+RTCVCC	+B +3VL	+5VALW +3VALW	+3VM +1.05VM	+1.5V +0.75V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +1.05VS +1.8VS
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

## Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

CONN@ : means ME part.

SV@ : means just build on SV Sku. LV Sku no build.

LV@ : means just build on LV Sku. SV Sku no build.

## Layout Notes

01/04 update

 : Question Area Mark.(Wait check)

**Install below 45 level BOM structure for ver. 0.1**

45@ : means just put it in the BOM of 45 level.

**Install below 43 level BOM structure for ver. 0.1**

DEBUG@ : means just build when PCIE port 80 CARD function enable. *Remove before MP*

## SMBUS Control Table

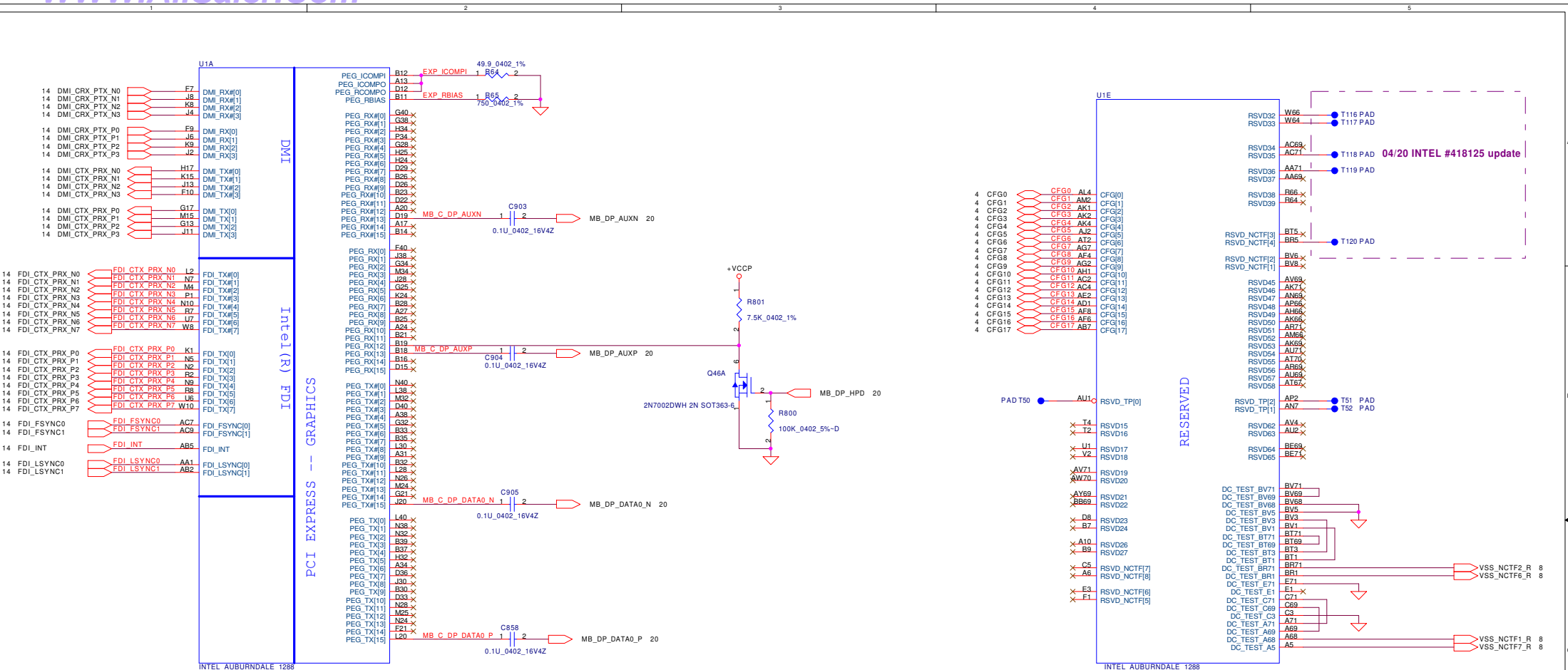
	SOURCE	BATT	XDP	SODIMM	CLK CHIP	MINI CARD	DOCK	NIC	THERMAL SENSOR	G-SENSOR
SMB_EC_CK1 SMB_EC_DAI	SMSC1098	V	X	X	X	X	X	X	X	X
SMBCLK SMBDATA	Calpella	X	V	V	V	V	V	X	X	V
SML0CLK SML0DATA	Calpella	X	X	X	X	X	X	V	X	X
SML1CLK SML1DATA	Calpella	X	X	X	X	X	X	X	V	V

## Strapping Options Flash

GNT1#	GNT0#	Routing
0	1	Reserved
1	0	Flash Cycles Routed to PCI
1	1	Flash Cycles Routed to SPI
0	0	Flash Cycles Routed to LPC

Security Classification	Compal Secret Data		Title	
Issued Date	2008/09/15	Deciphered Date	2010/12/31	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. IT IS NOT TO BE REPRODUCED, COPIED, TRANSMITTED, OR OTHERWISE DISCLOSED TO ANY OTHER PERSON OR ENTITY WITHOUT THE WRITTEN PERMISSION OF COMPAL ELECTRONICS, INC. THE INFORMATION IT CONTAINS IS NOT TO BE USED FOR ANY PURPOSES OTHER THAN THE SPECIFIC PURPOSE FOR WHICH IT WAS PROVIDED TO YOU BY COMPAL ELECTRONICS, INC.				Notes List
Size	Document Number	Rev		
Custody	LA-525IP	0.9		
Date:	Tuesday, January 05, 2010	Sheet	3	of 47





## CFG Straps for PROCESSOR

**CFG0** R68 1 2 @3.01K 0402 1%

PCI-Express Configuration Select  
1: Single PEG  
0: Bifurcation enabled  
Not applicable for Clarkfield Processor

**CFG3** R69 1 2 @3.01K 0402 1%

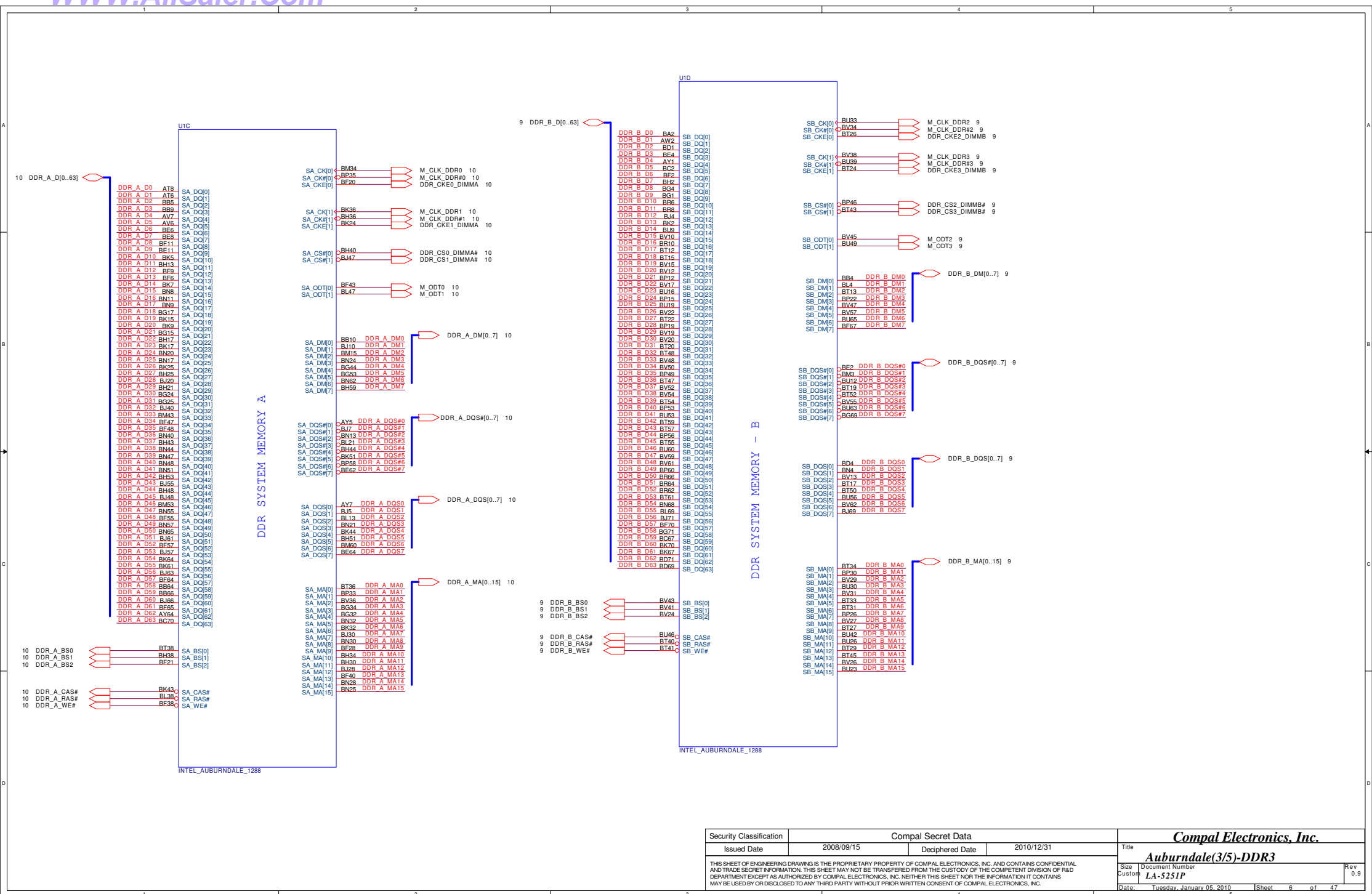
CFG3-PCI Express Static Lane Reversal  
1: Normal Operation  
0: Lane Numbers Reversed  
15 -> 0, 14 -> 1, .....

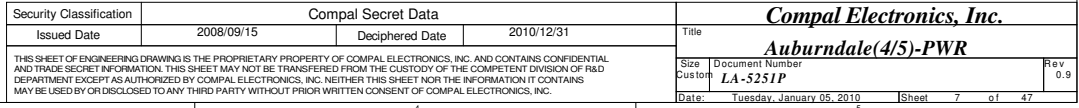
**CFG4** R70 1 2 3.01K 0402 1%

**ES1 sample need negative voltage**  
**ES2 sample contact to GND**

CFG4-Display Port Presence  
1: Disabled; No Physical Display Port attached to Embedded Display Port  
0: Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification	Compal Secret Data		Title
Issued Date	2008/09/15	Deciphered Date	2010/12/31
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			<b>Compal Electronics, Inc.</b> <b>Auburndale(2/5)-DMI/PEG/FDI</b> Size: Document Number Custom: LA-5251P Date: Tuesday, January 05, 2010 Sheet 5 of 47





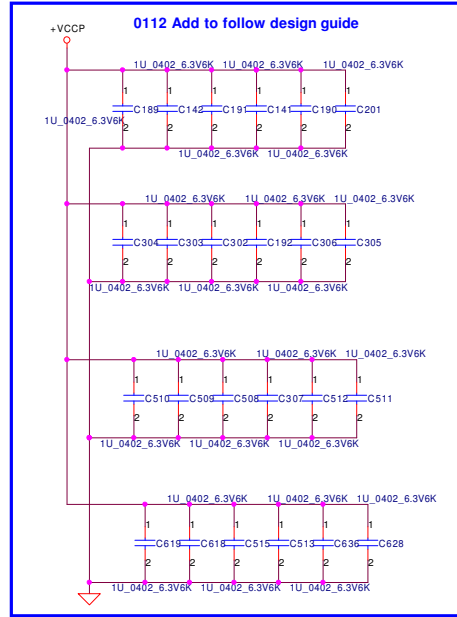
U11		AY24
BU62	VSS1	VSS90
BU68	VSS2	VSS91
BU65	VSS3	VSS92
BU61	VSS4	VSS93
BU48	VSS5	VSS94
BU44	VSS6	VSS95
BU37	VSS7	VSS96
BU32	VSS8	VSS97
BU25	VSS9	VSS98
BU21	VSS10	VSS99
BU18	VSS11	VSS100
BU14	VSS12	VSS101
BU11	VSS13	VSS102
BP42	VSS14	VSS103
BN64	VSS15	VSS104
BN6	VSS16	VSS105
BM70	VSS17	VSS106
BM51	VSS18	VSS107
BM44	VSS19	VSS108
BM2	VSS20	VSS109
BM24	VSS21	VSS110
BM17	VSS22	VSS111
BL57	VSS23	VSS112
BL55	VSS24	VSS113
BL40	VSS25	VSS114
BL28	VSS26	VSS115
BL20	VSS27	VSS116
BK63	VSS28	VSS117
BK60	VSS29	VSS118
BK53	VSS30	VSS119
BK34	VSS31	VSS120
BK10	VSS32	VSS121
BJ64	VSS33	VSS122
BJ21	VSS34	VSS123
BJ8	VSS35	VSS124
BJ1	VSS36	VSS125
BH70	VSS37	VSS126
BH57	VSS38	VSS127
BH45	VSS39	VSS128
BH47	VSS40	VSS129
BH24	VSS41	VSS130
BH20	VSS42	VSS131
BH15	VSS43	VSS132
BG51	VSS44	VSS133
BG36	VSS45	VSS134
BG2	VSS46	VSS135
BF30	VSS47	VSS136
BF13	VSS48	VSS137
BF3	VSS49	VSS138
BE70	VSS50	VSS139
BE65	VSS51	VSS140
BE9	VSS52	VSS141
BE1	VSS53	VSS142
BD57	VSS54	VSS143
BD63	VSS55	VSS144
BD60	VSS56	VSS145
BD46	VSS57	VSS146
BD42	VSS58	VSS147
BD39	VSS59	VSS148
BD14	VSS60	VSS149
BB71	VSS61	VSS150
BB62	VSS62	VSS151
BB57	VSS63	VSS152
BB56	VSS64	VSS153
BB50	VSS65	VSS154
BB46	VSS66	VSS155
BB42	VSS67	VSS156
BB39	VSS68	VSS157
BB7	VSS69	VSS158
BB1	VSS70	VSS159
BA70	VSS71	VSS160
AY71	VSS72	VSS161
AY66	VSS73	VSS162
AY62	VSS74	VSS163
AY59	VSS75	VSS164
AY55	VSS76	VSS165
AY51	VSS77	VSS166
AY48	VSS78	VSS167
AY42	VSS79	VSS168
AR39	VSS80	VSS169
AR35	VSS81	VSS170
AR33	VSS82	VSS171
AR24	VSS83	VSS172
AR20	VSS84	VSS173
AR17	VSS85	VSS174
AR15	VSS86	VSS175
AR14	VSS87	VSS176
AR4	VSS88	VSS177
AR1	VSS89	VSS178
AP70	VSS90	VSS179
AP64	VSS91	VSS180
AN62	VSS92	VSS181
AN55	VSS93	VSS182
AY44	VSS94	VSS183
AY41	VSS95	VSS184
AY37	VSS96	VSS185
AY35	VSS97	VSS186
AY33	VSS98	VSS187
AY32	VSS99	VSS188
AY30	VSS100	VSS189
AY28	VSS101	VSS190
AY26	VSS102	VSS191

VSS

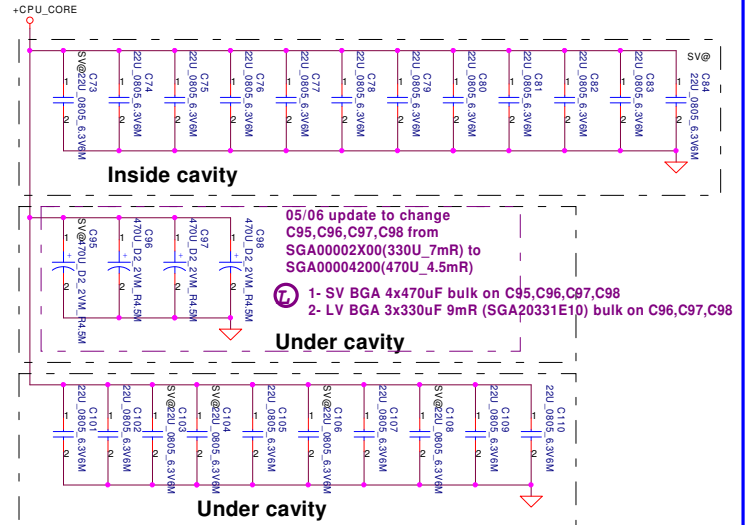
VSS

INTEL\_AUBURNDAL5\_1288

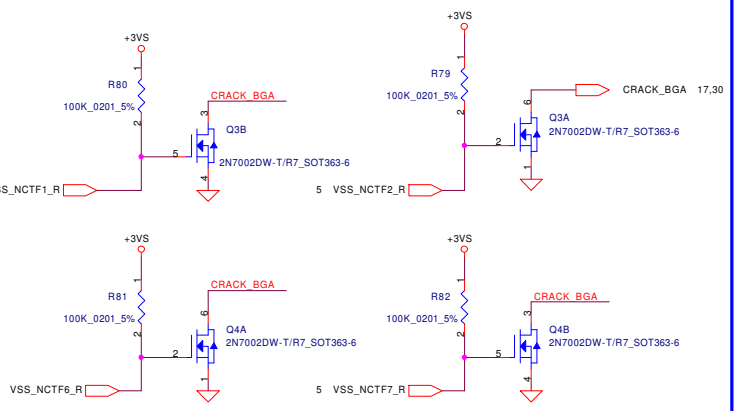
INTEL\_AUBURNDAL5\_1288



## CPU CORE

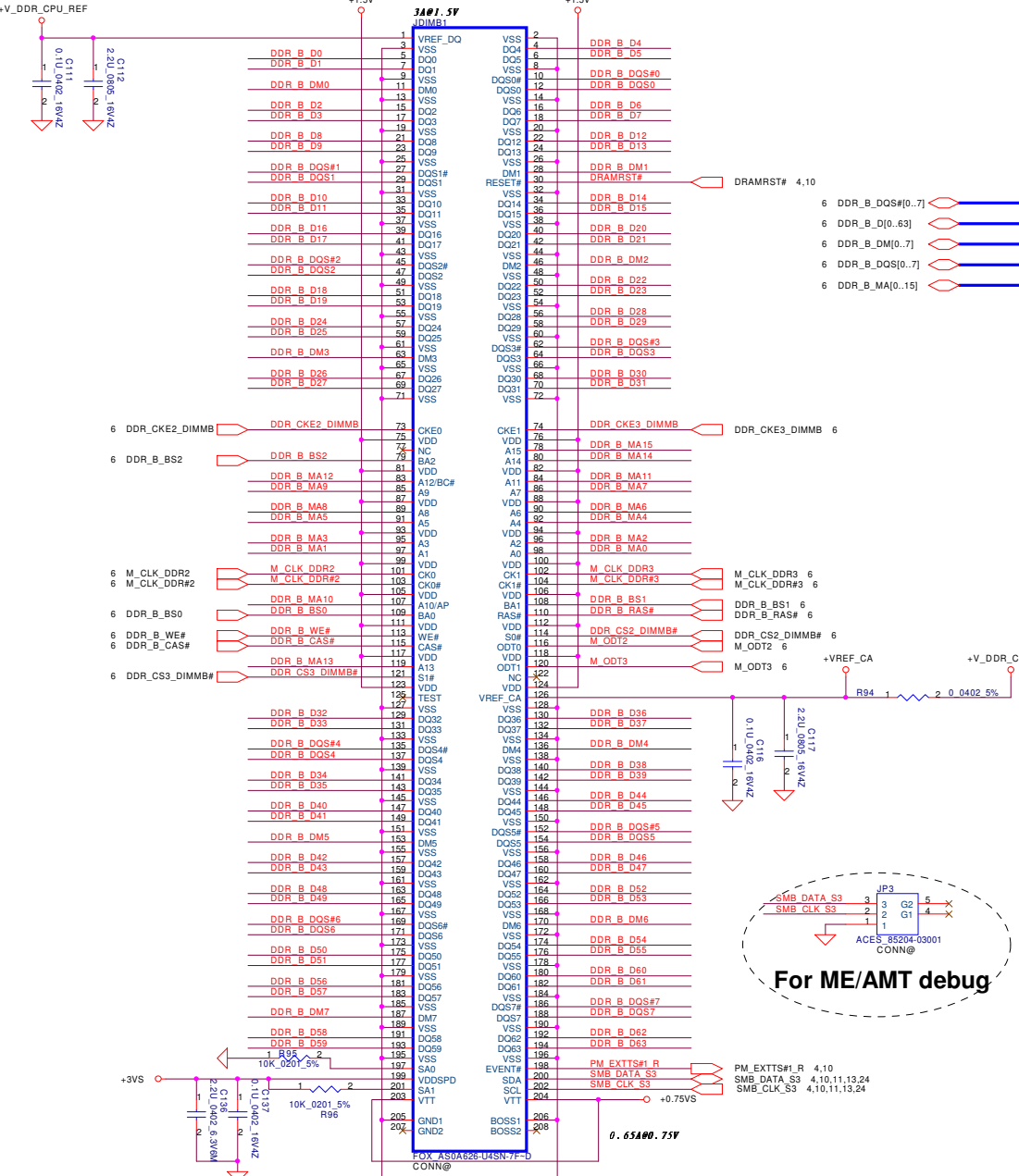


## BGA Ball Cracking Prevention and Detection



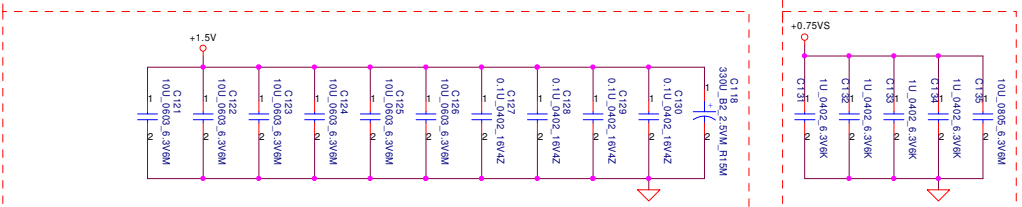
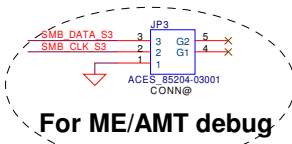
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/09/15	Deciphered Date	2010/12/31	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				
Title	Auburndale(5/5)-GND/Bypass		Size	Document Number
Customer	LA-5251P		Rev	0.9
Date	Tuesday, January 05, 2010	Sheet	8	of 47

# DDR3 SO-DIMM B



Layout Note:  
Place near JDIMB1

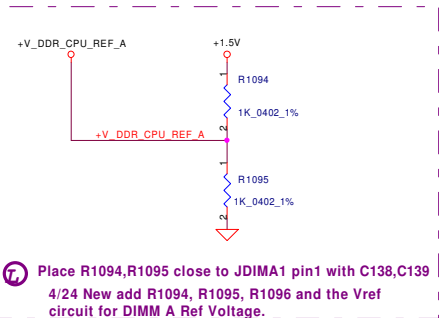
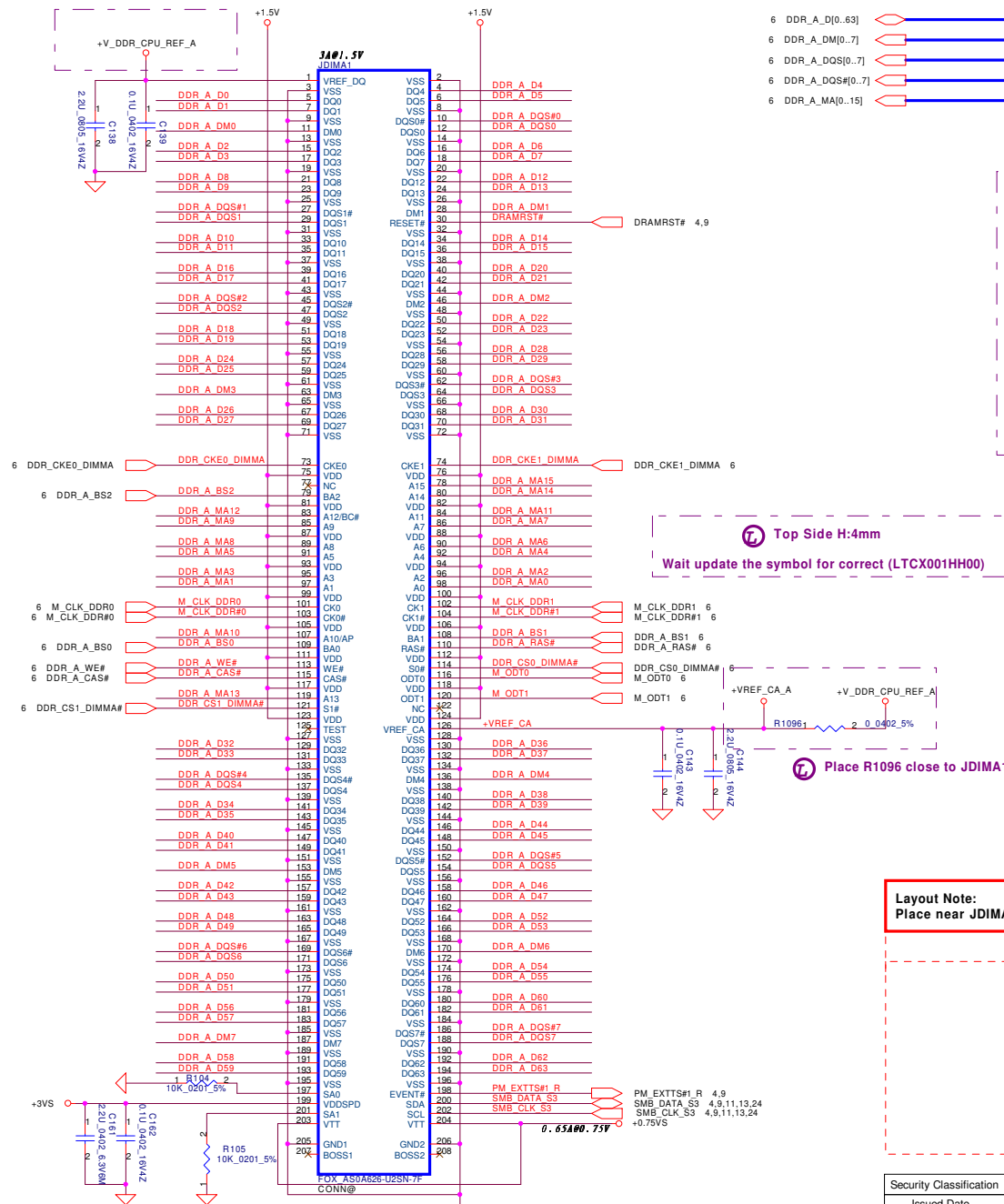
Layout Note:  
Place near JDIMB1



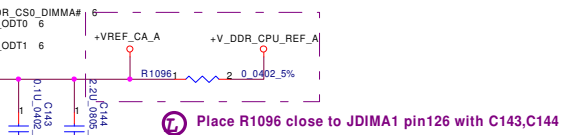
Bottom Side H:5.2mm  
Wait update the symbol for correct (LTCX001HL00)

Security Classification		Compal Secret Data		Title	
Issued Date	2008/09/15	Deciphered Date	2010/12/31	DDR3-SODIMM SLOT1	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Size		Document Number	Rev
Custom		LA-5251P		0.9	
Date:		Tuesday, January 05, 2010		Sheet	9 of 47

# DDR3 SO-DIMM A

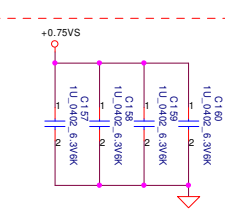
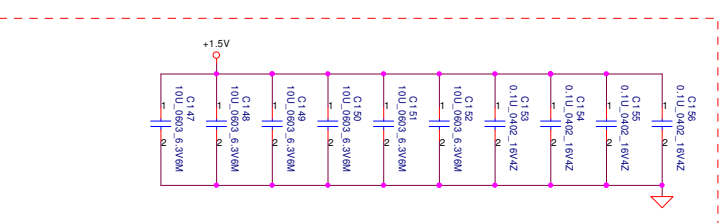


**Top Side H:4mm**  
**Wait update the symbol for correct (LTCX001HH00)**

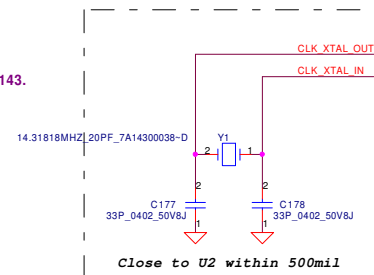
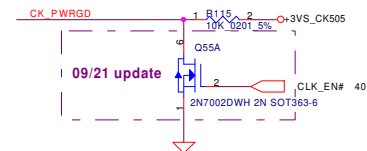
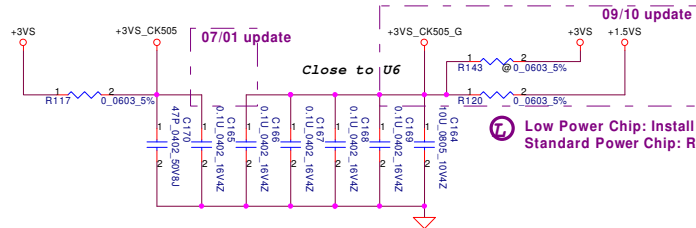
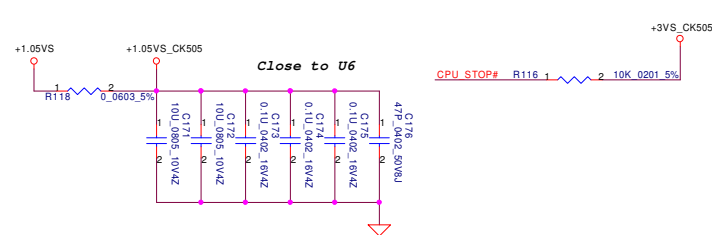
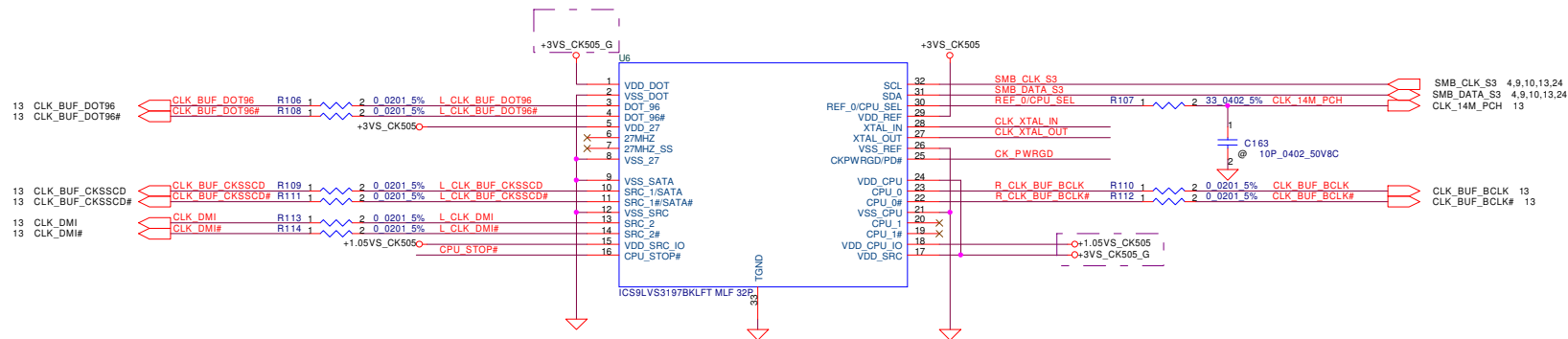


**Layout Note:**  
**Place near JDIMA1**

**Layout Note:**  
**Place near JDIMA1**

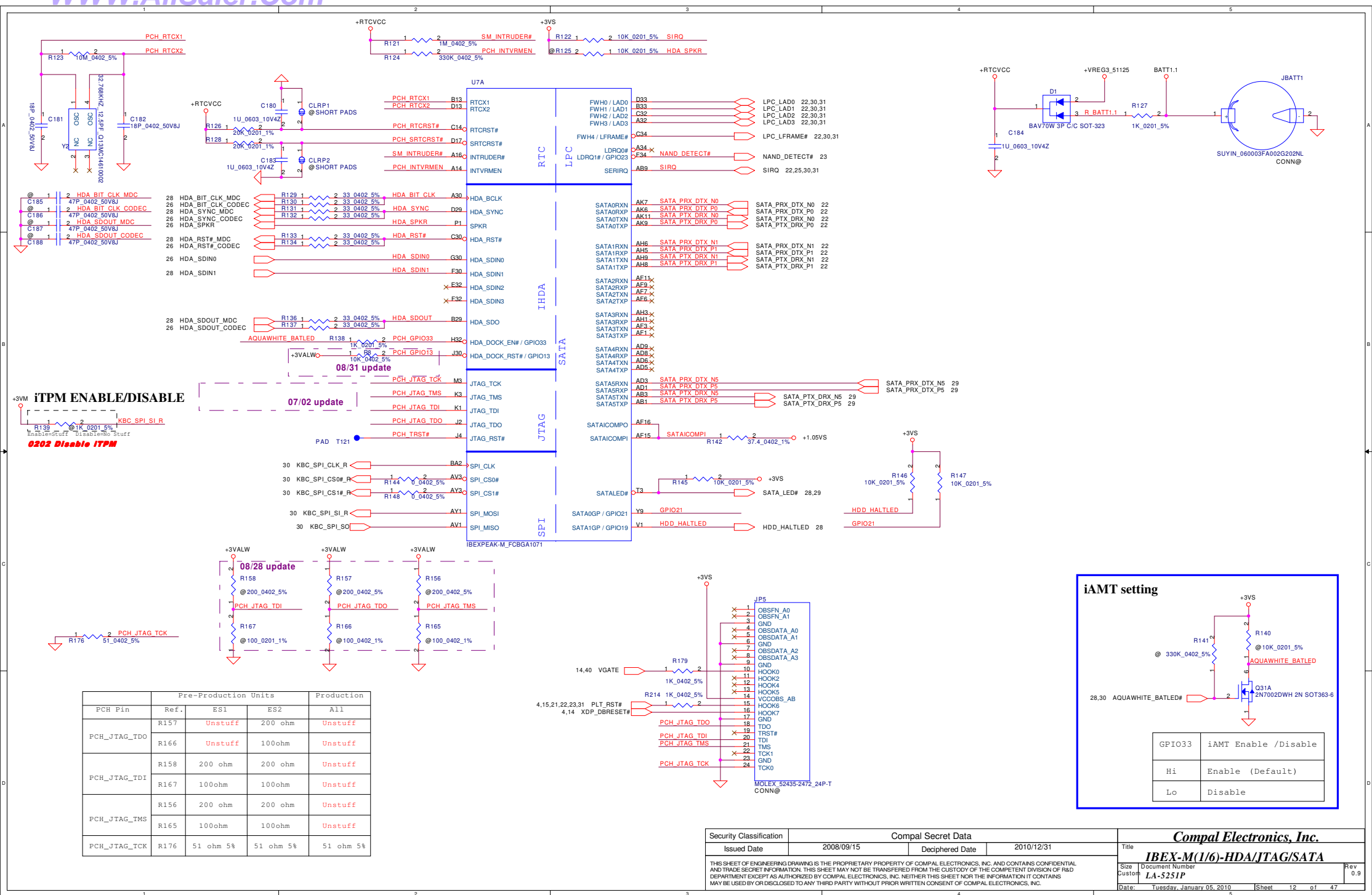


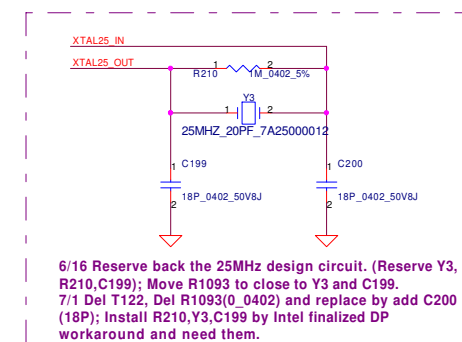
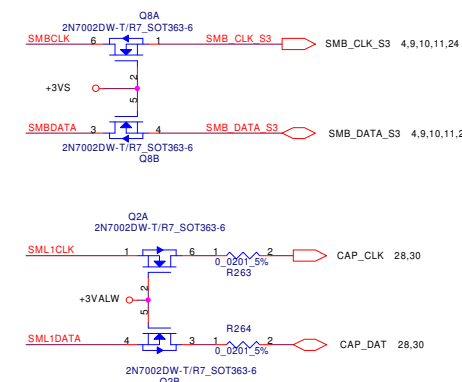
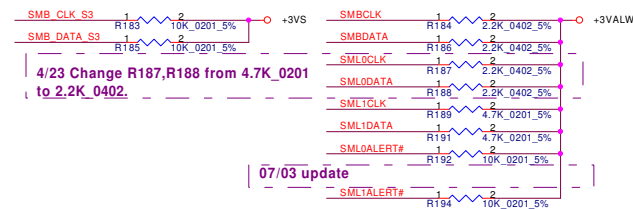
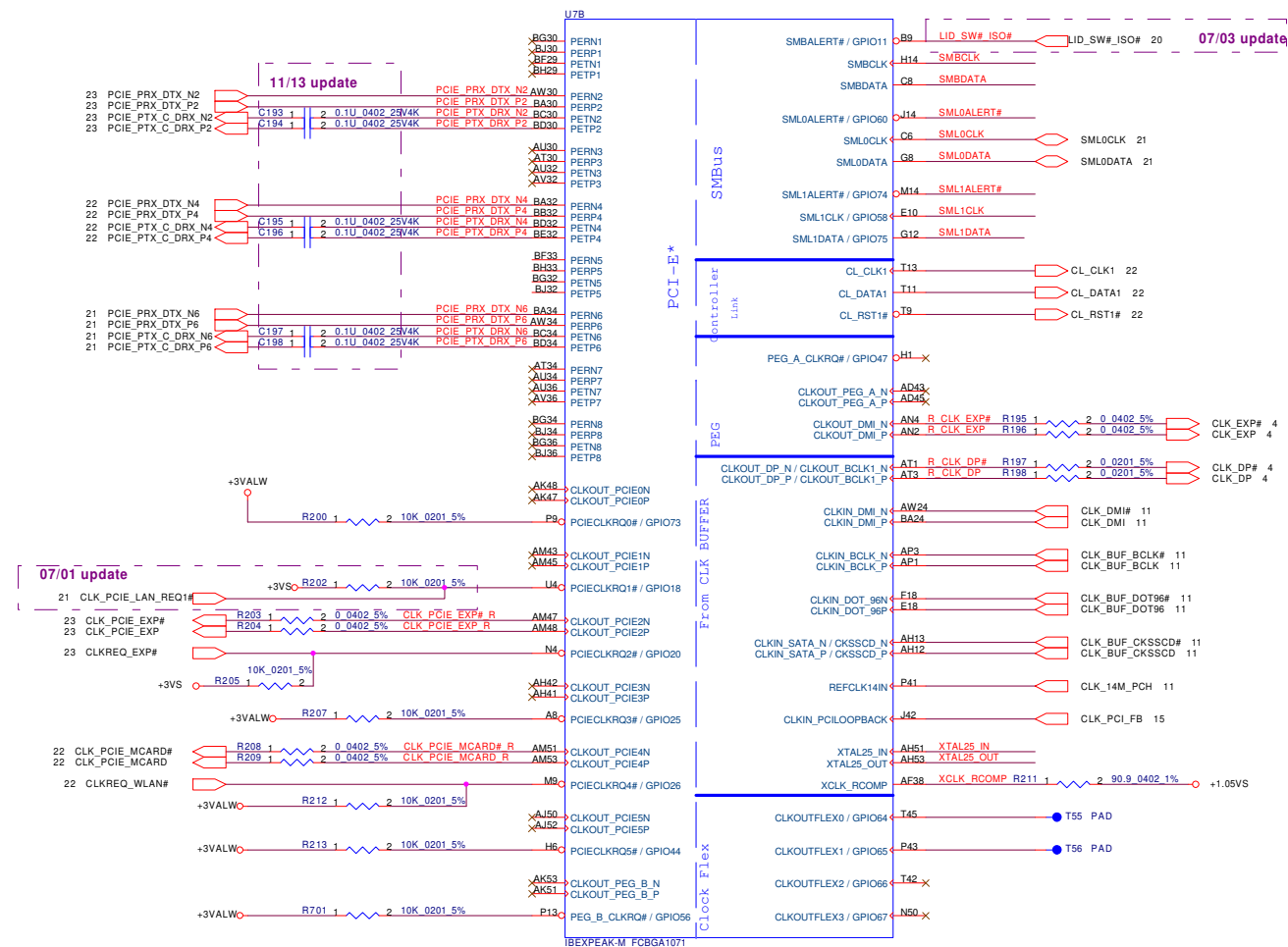
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/09/15	Deciphered Date	2010/12/31	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				DDR3-SODIMM SLOT2	
Size		Document Number		Rev	
		LA-5251P		0.9	
Date:		Tuesday, January 05, 2010		Sheet	
				10 of 47	



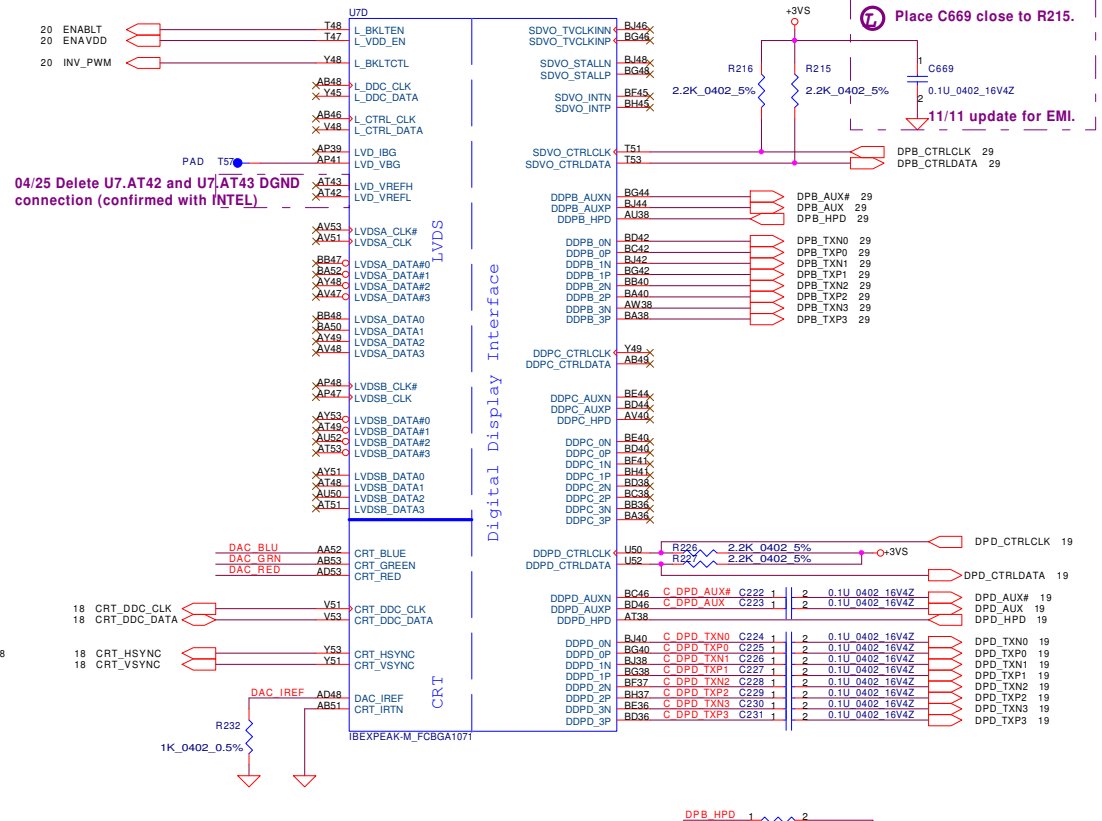
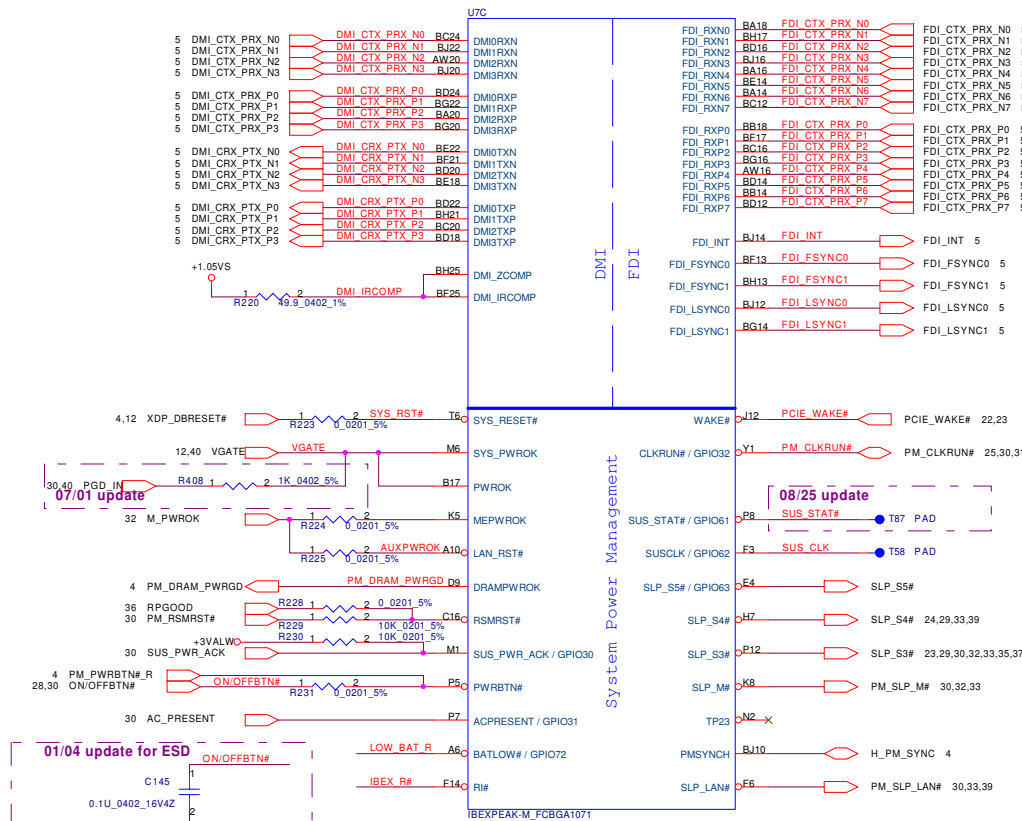
Low Power Chip: Install R120 and remove R143.  
Standard Power Chip: Remove R120 and Install R143.

Security Classification		Compal Secret Data		Title	
Issued Date	2008/09/15	Deciphered Date	2010/12/31	CLOCK GENERATOR	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				LA-5251P	Rev 0.9
Date:				Tuesday, January 05, 2010	Sheet 11 of 47

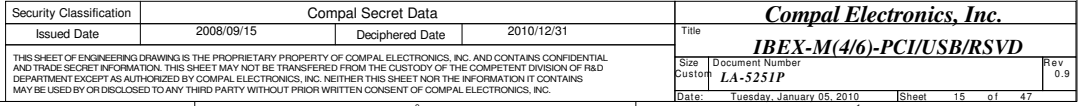


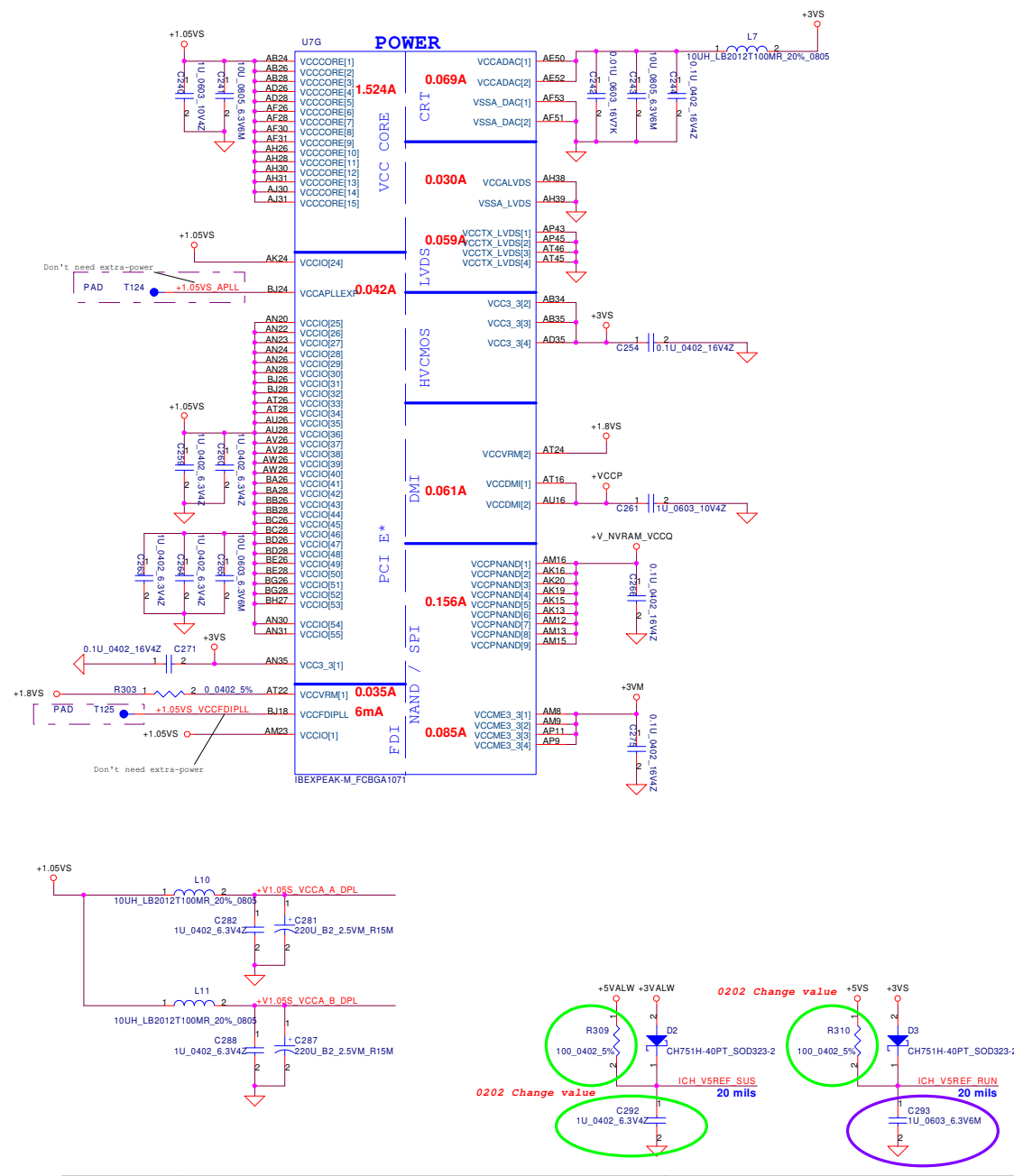
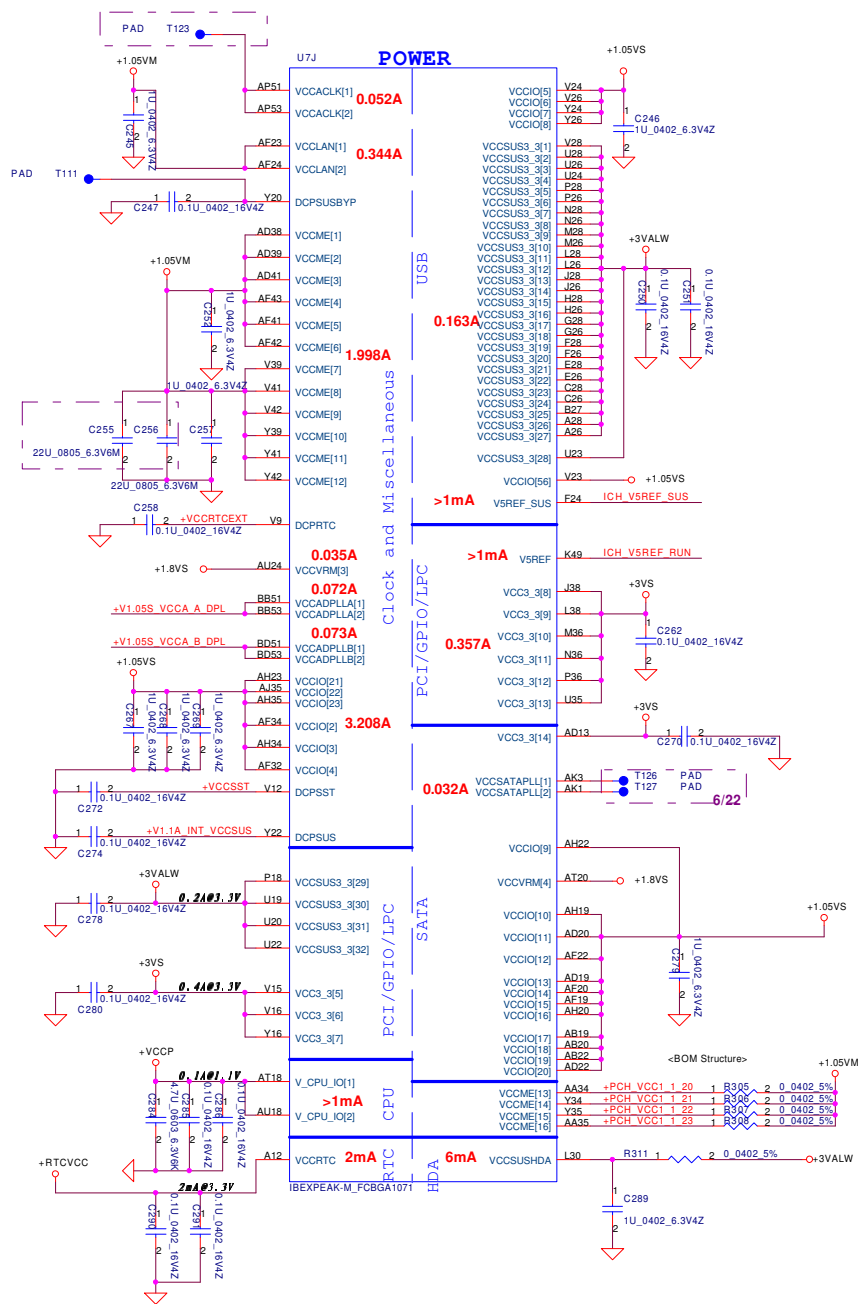


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/09/15	Deciphered Date	2010/12/31	Title	IBEX-M(2/6)-PCI-E/SMBUS/CLK
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	LA-5251P
				Date	Tuesday, January 05, 2010
				Sheet	13 of 47
				Rev	0.9

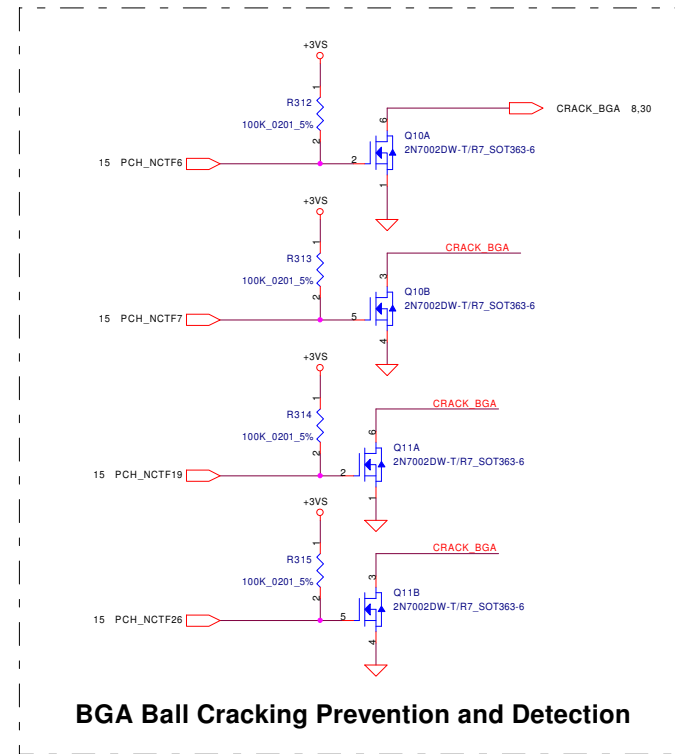
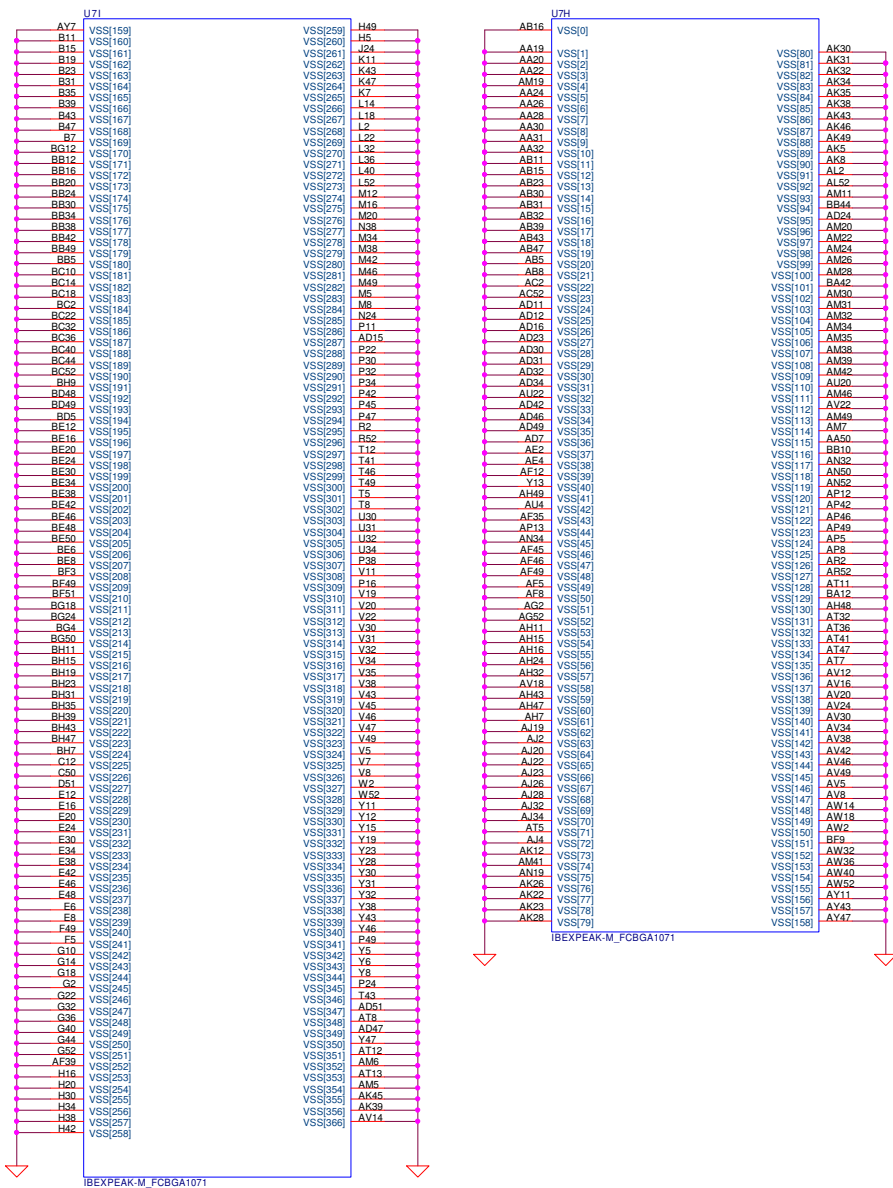


Security Classification		Compal Secret Data		Title	
Issued Date	2008/09/15	Deciphered Date	2010/12/31	IBEX-M(3/6)-DMI/GPIO/LVDS	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. IT IS TO BE KEPT UNDER THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS IS TO BE REPRODUCED, COPIED, OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	LA-5251P
				Date:	Tuesday, January 05, 2010
				Sheet	14 of 47



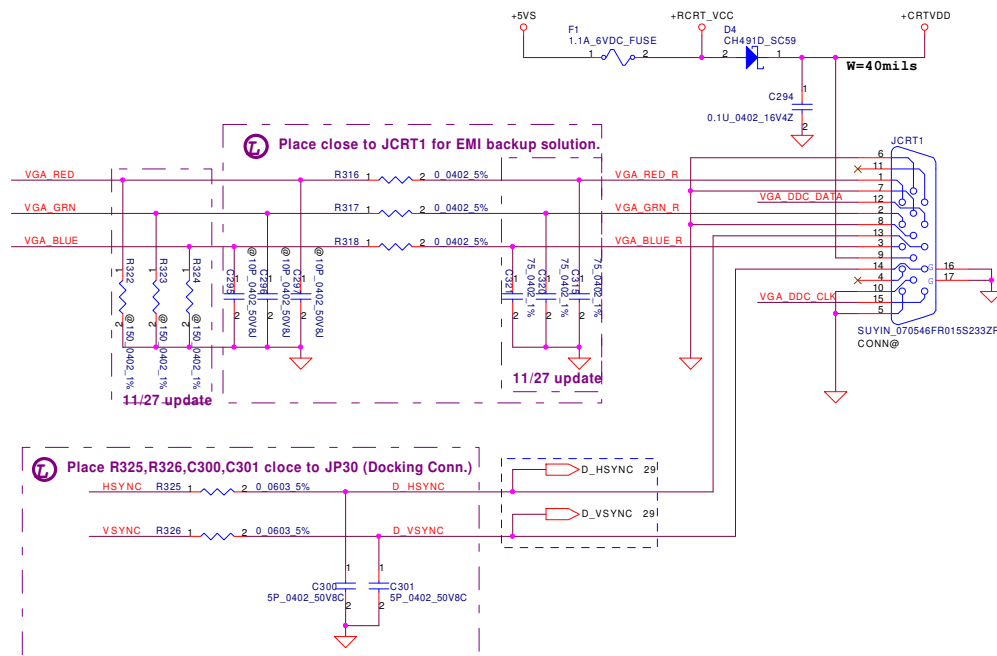
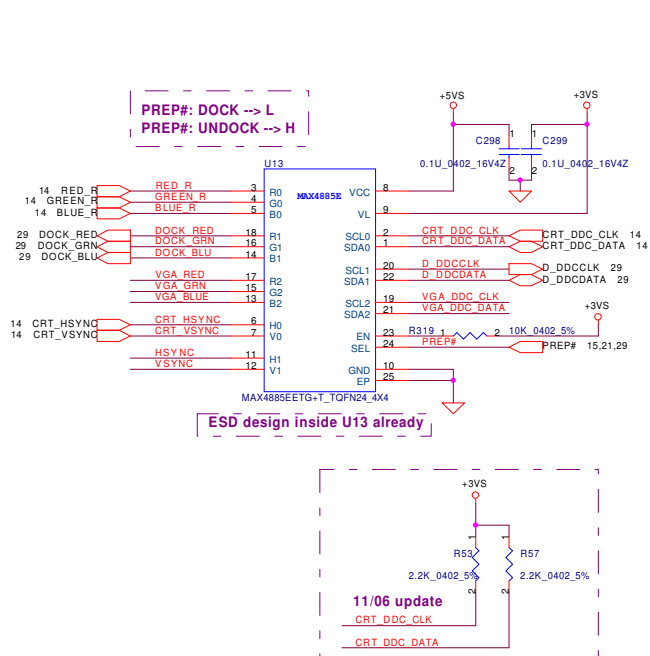


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/09/15	Deciphered Date	2010/12/31	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				IBEX-M(5/6)-PWR
Size	Document Number	Rev	0.9	
Custom	LA-5251P	Date	Tuesday, January 05, 2010	Sheet 16 of 47

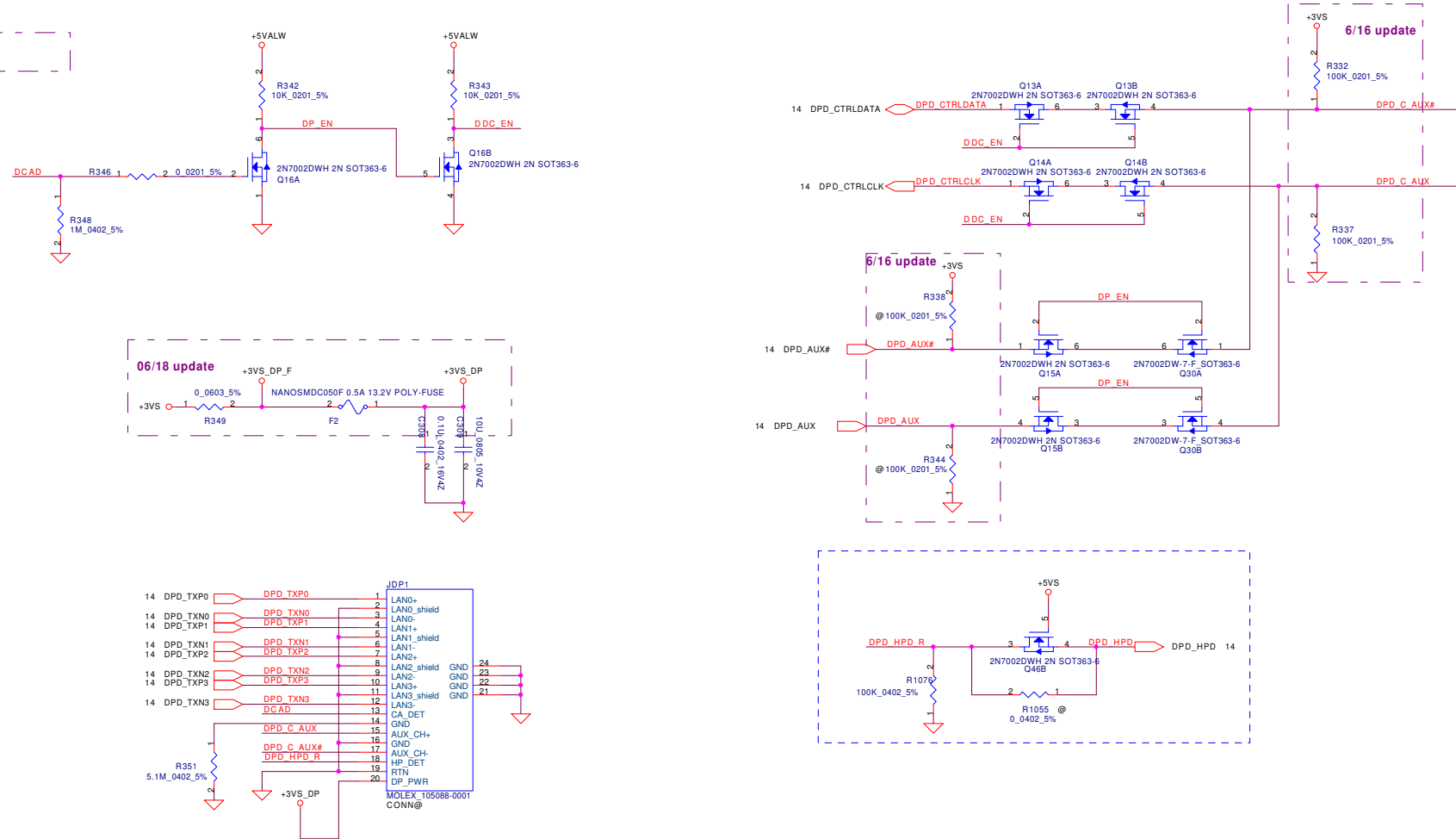


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/09/15	Deciphered Date	2010/12/31	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				IBEX-M(6/6)-GND
Size	Document Number	Rev		
Custom	LA-5251P	0.9		
Date:	Tuesday, January 05, 2010	Sheet	17	of 47

# CRT Connector

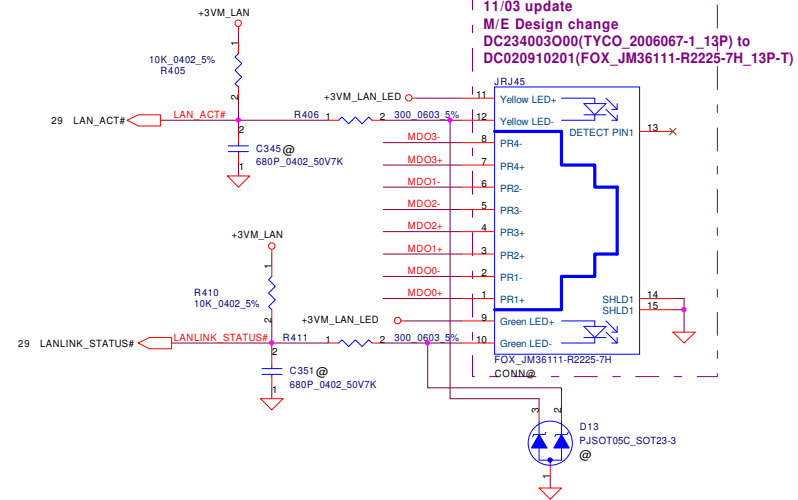
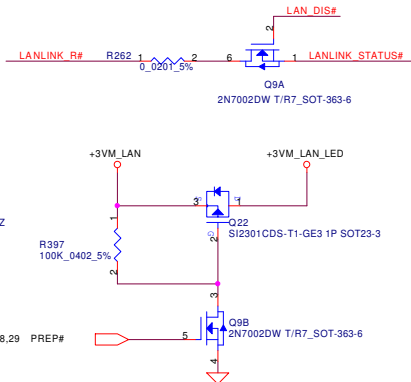
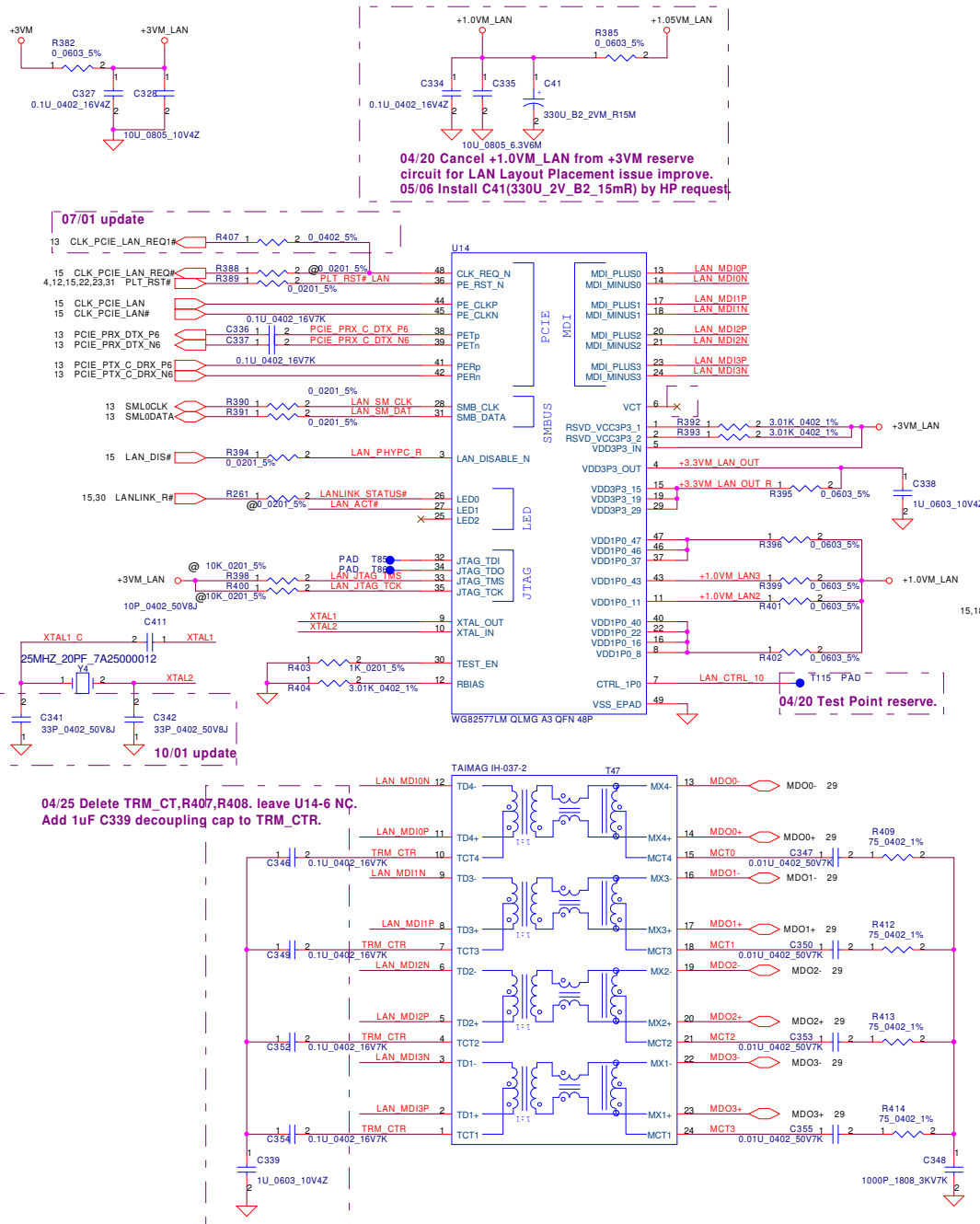


Security Classification	Compal Secret Data		Title	
Issued Date	2008/09/15	Deciphered Date	2010/12/31	Compal Electronics, Inc.
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				CRT Connector
Size	Document Number	Rev		0.9
LA-5251P		Date: Tuesday, January 05, 2010 Sheet 18 of 47		

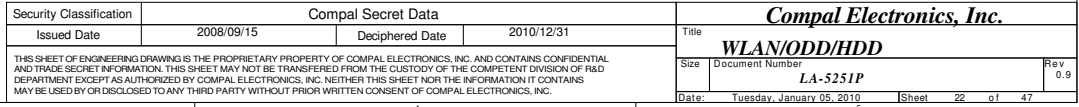


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/09/15	Deciphered Date	2010/12/31	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number
				LA-5251P
				Rev
				0.9
Date: Tuesday, January 05, 2010		Sheet 19 of 47		



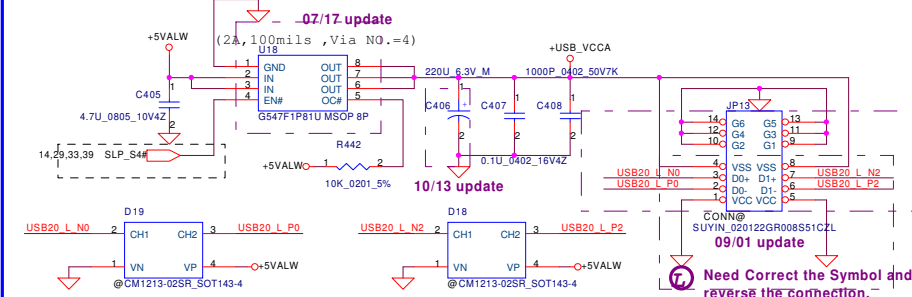


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/09/15	Deciphered Date	2010/12/31	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Intel 82566 Nineveh	
Size		Document Number		Rev	
LA-5251P		LA-5251P		0.9	
Date:		Tuesday, January 05, 2010		Sheet	21 of 47

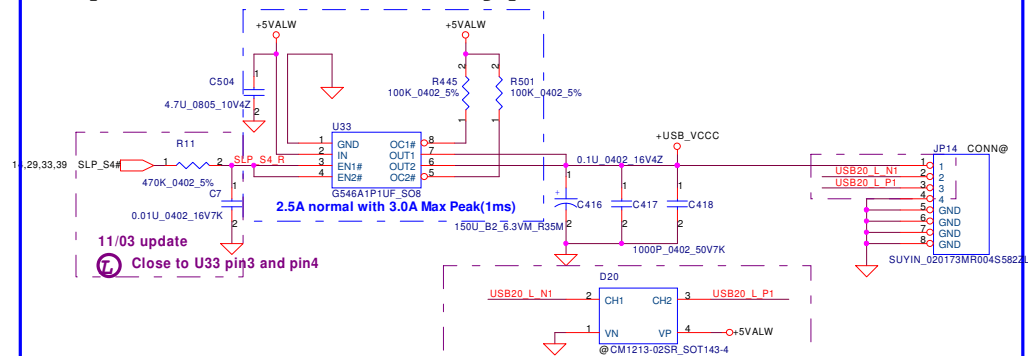




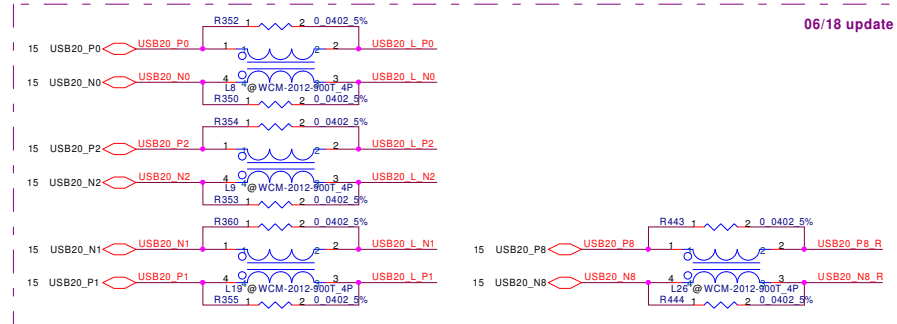
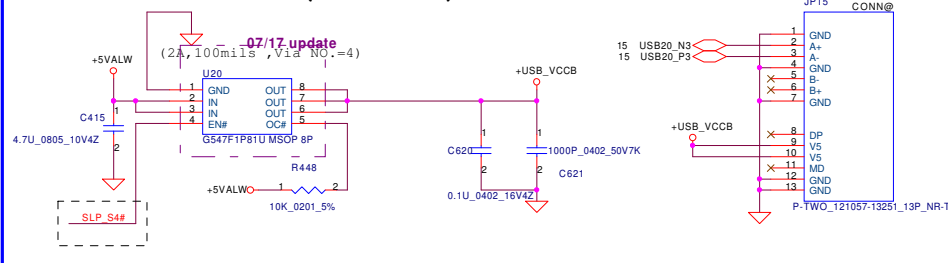
## Rear side USB conn.



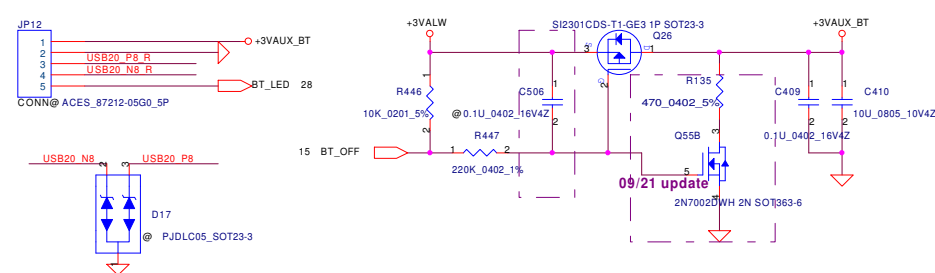
## USB+power conn. (Left Side)-debug port



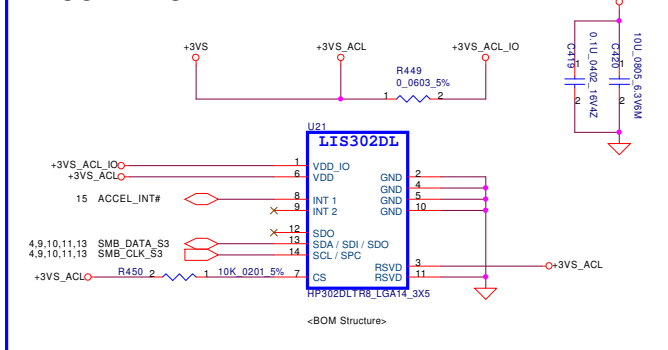
## Left side USB conn. (Extra-USB)



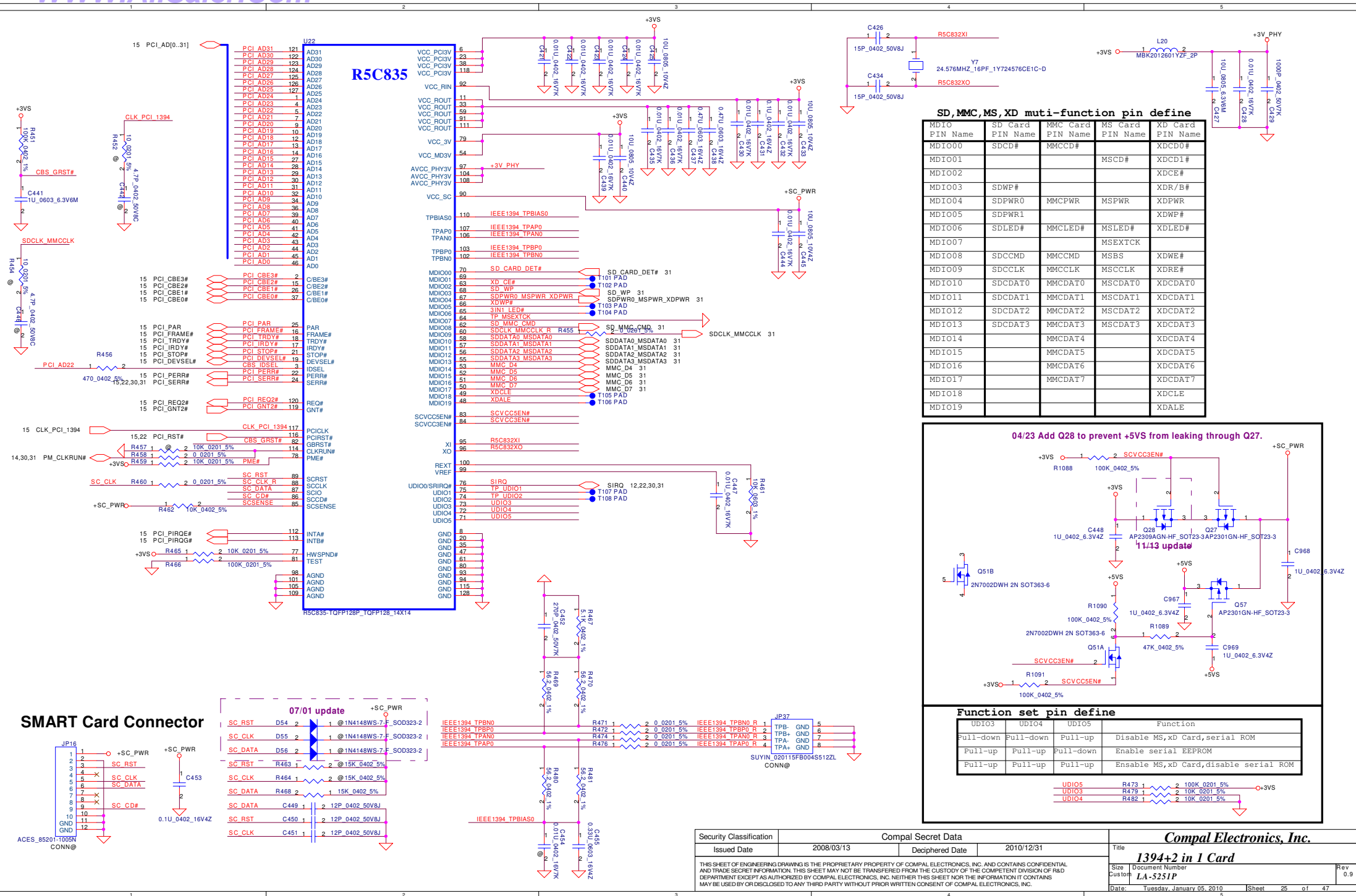
## BT Connector

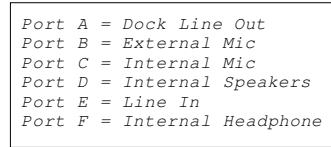


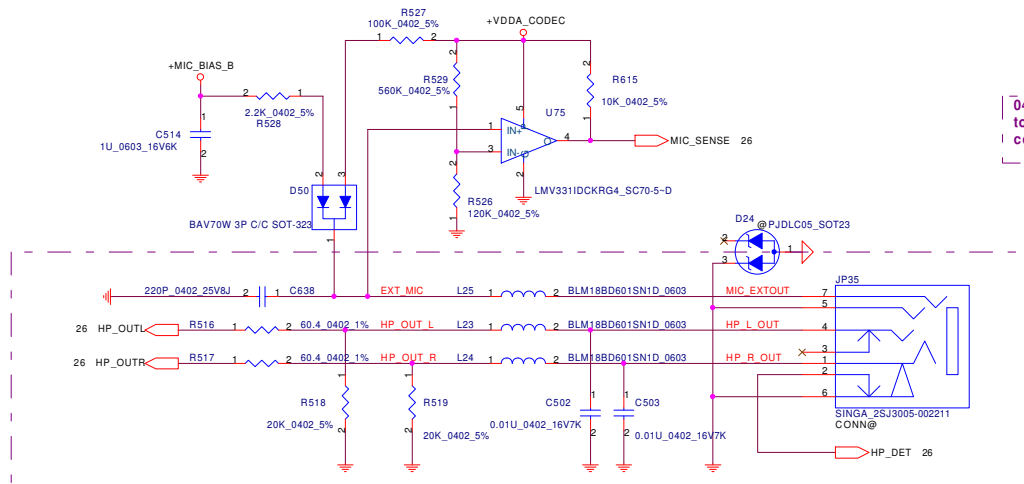
## ACCELEROMETER



Security Classification	Compal Secret Data		Title	
Issued Date	2008/09/15	Deciphered Date	2010/12/31	USB & BT Connector & Accelerometer
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size
				Document Number
				LA-5251P
				Rev
				0.9
				Date
				Tuesday, January 05, 2010
				Sheet
				24 of 47

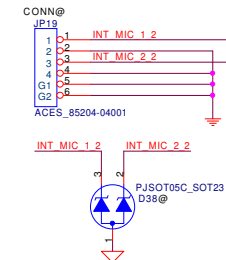




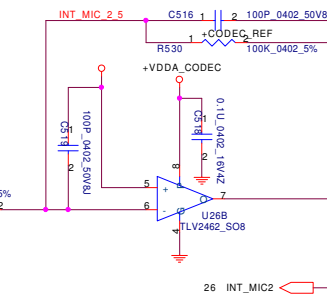
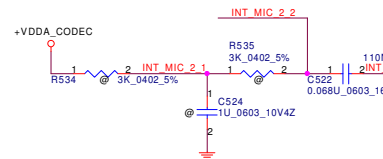
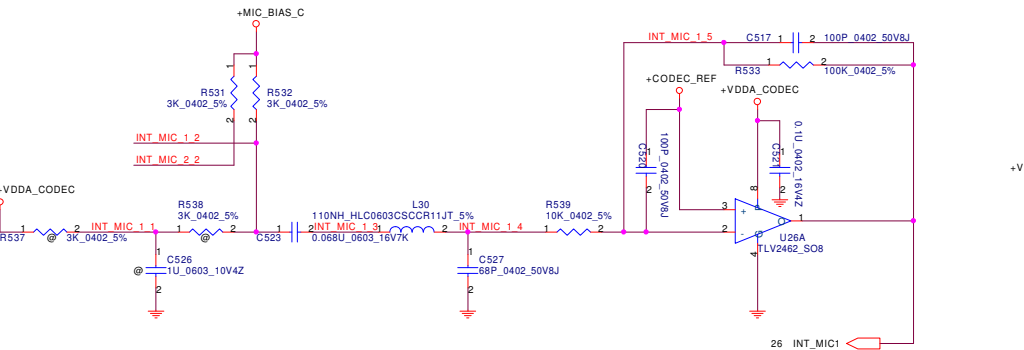
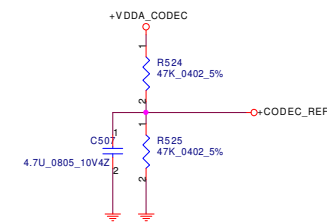
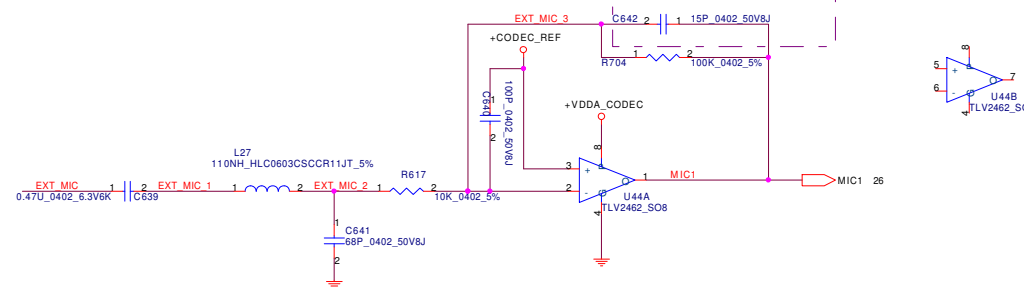


04/24 Correct the Symbol from SINGA\_2SJ-B960-003 to SINGA\_2SJ3005-002211, also correct the connection for fix Audio work abnormal issue.

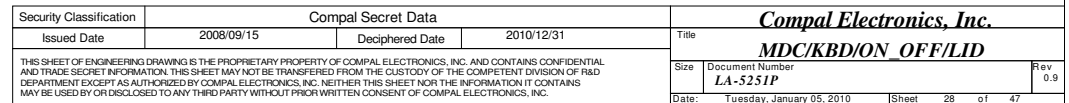
Old	New
1HP_L_OUT	1HP_R_OUT
2HP_R_OUT	2HP_DET
3GNDA	3DUMMY net
4MIC_EXTOUT	4HP_L_OUT
5DUMMY net	5GNDA
6HP_DET	6GNDA
7GNDA	7MIC_EXTOUT

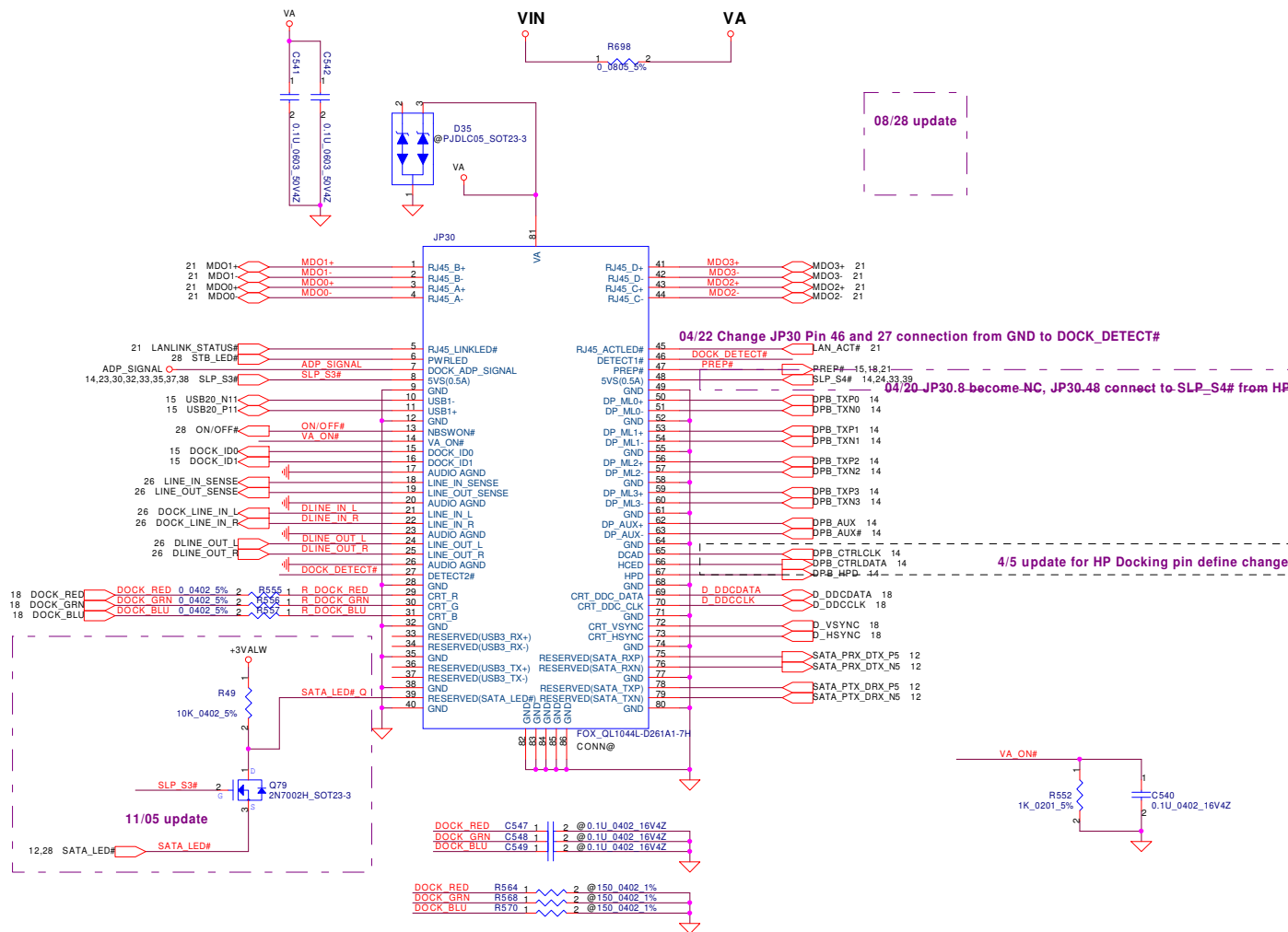


04/27 Change C642 from 33P to 15P via IDT recommend to fix the SVTP fail issue.

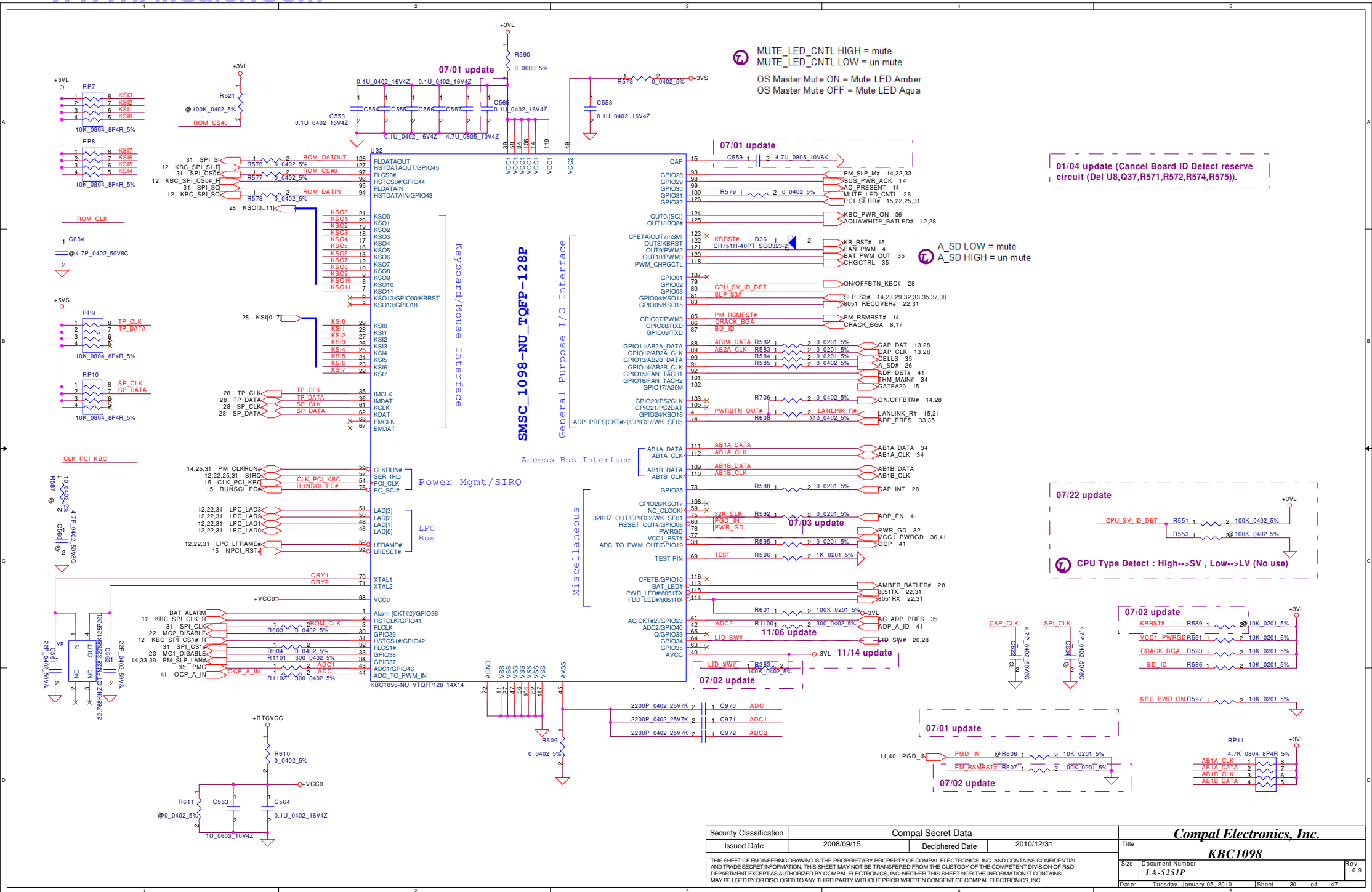


Security Classification	Compal Secret Data		Title	
Issued Date	2008/09/15	Deciphered Date	2010/12/31	Compal Electronics, Inc.
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				AMP & Audio Jack
Size	Document Number	Rev		0.9
LA-5251P	Tuesday, January 05, 2010		Sheet	27 of 47

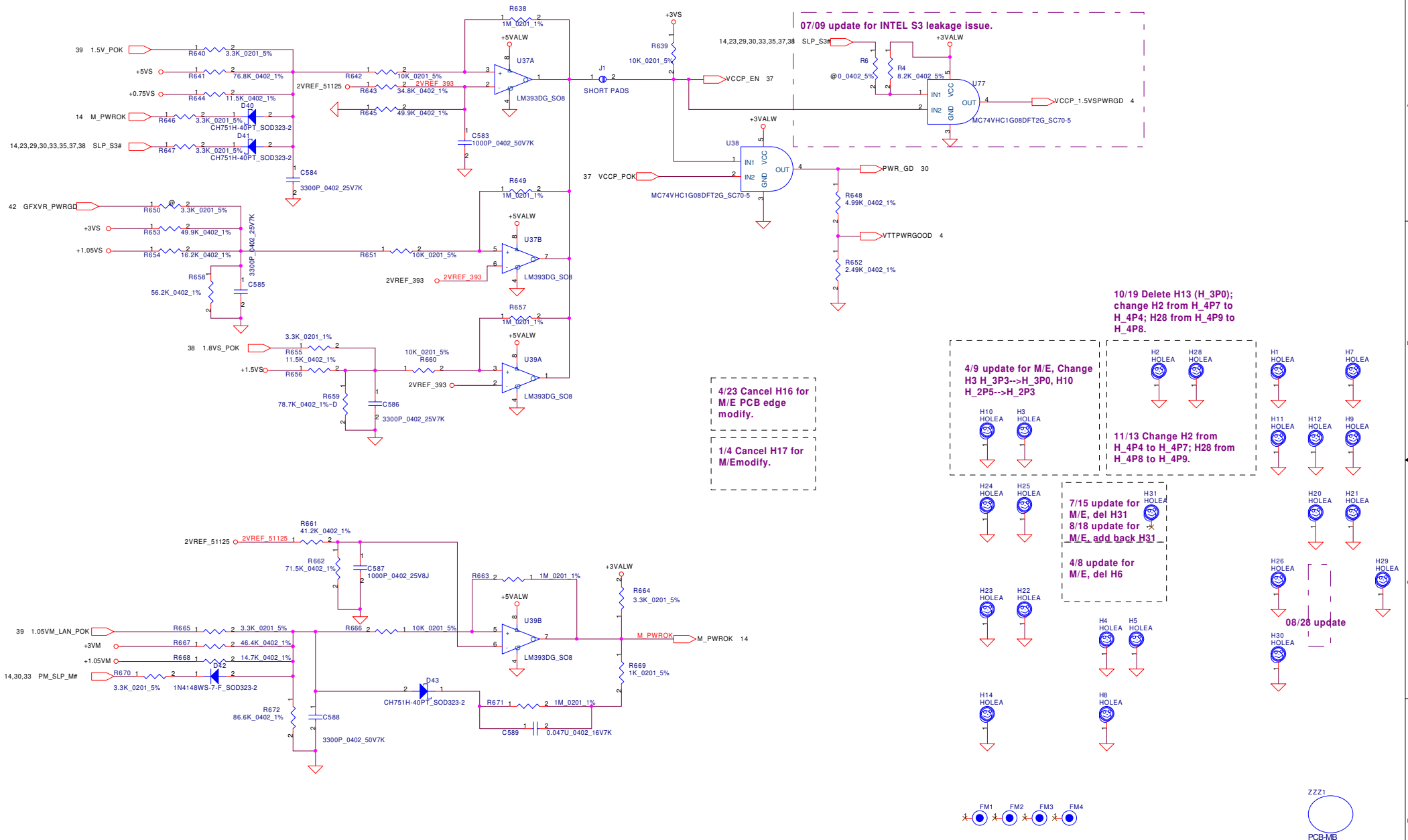




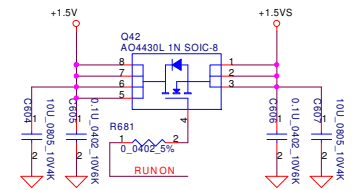
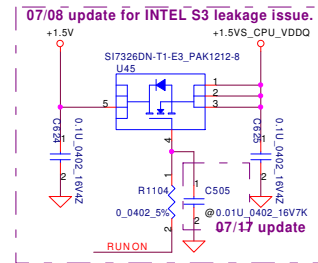
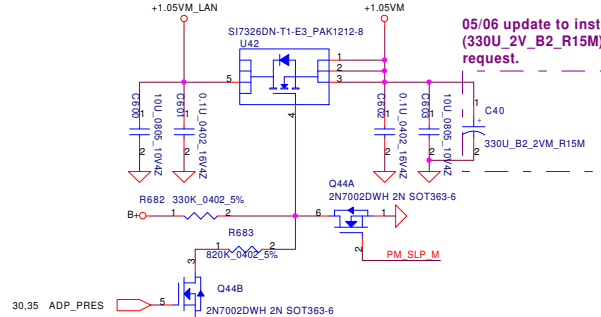
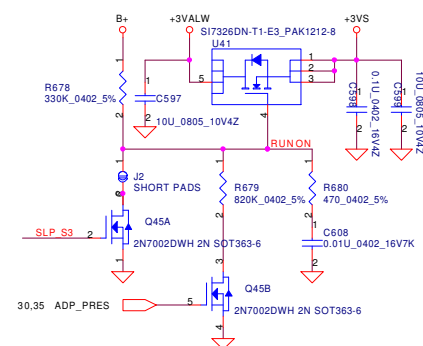
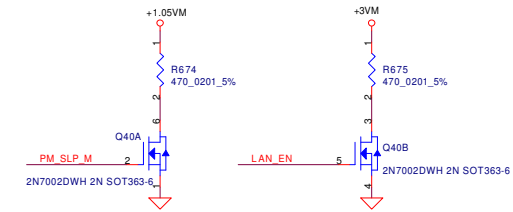
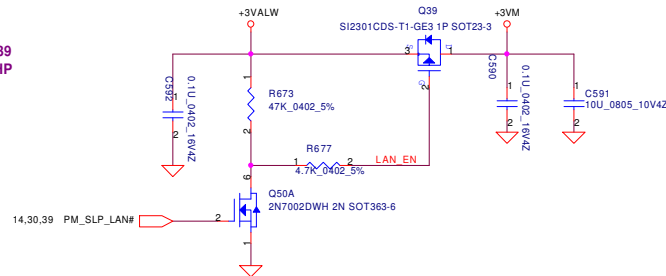
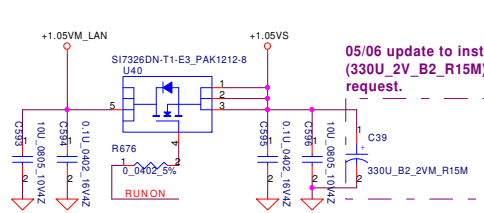
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/09/15	Deciphered Date	2010/12/31	Title	DOCK_CONN
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	LA-5251P
				Rev	0.9
Date: Tuesday, January 05, 2010				Sheet	29 of 47



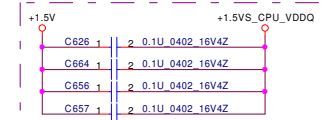




Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/09/15	Deciphered Date	2010/12/31	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				POK CKT
Size	Document Number	Rev	Date: Tuesday, January 05, 2010	
LA-5251P	0.9	32	Sheet 32 of 47	

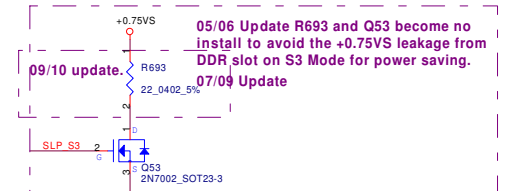
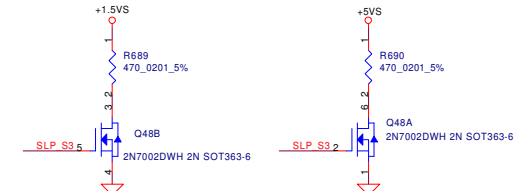
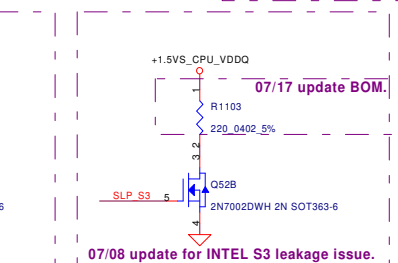
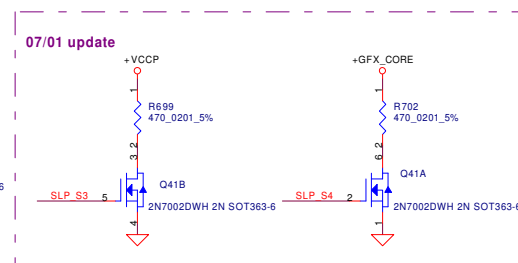
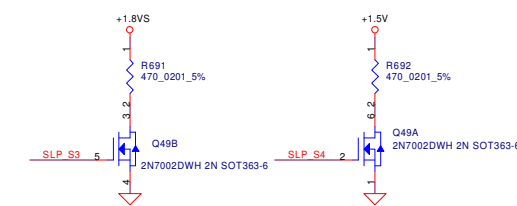
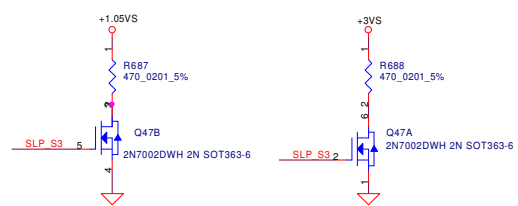
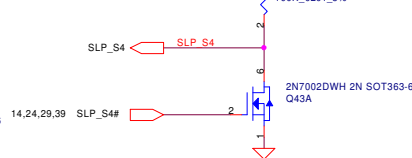
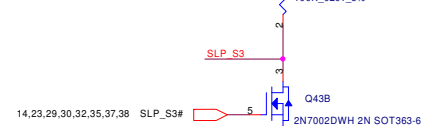
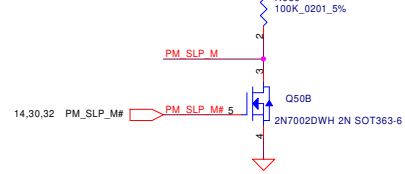
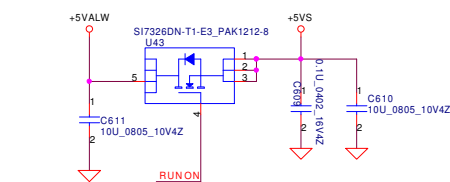
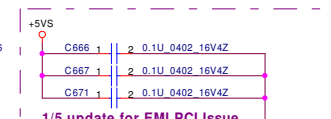


⚙ Add C626,C664 close to JDIMA1;  
C656,C657 close to JDIMB1.

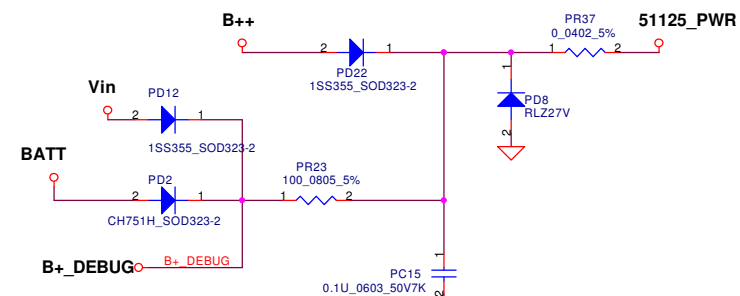
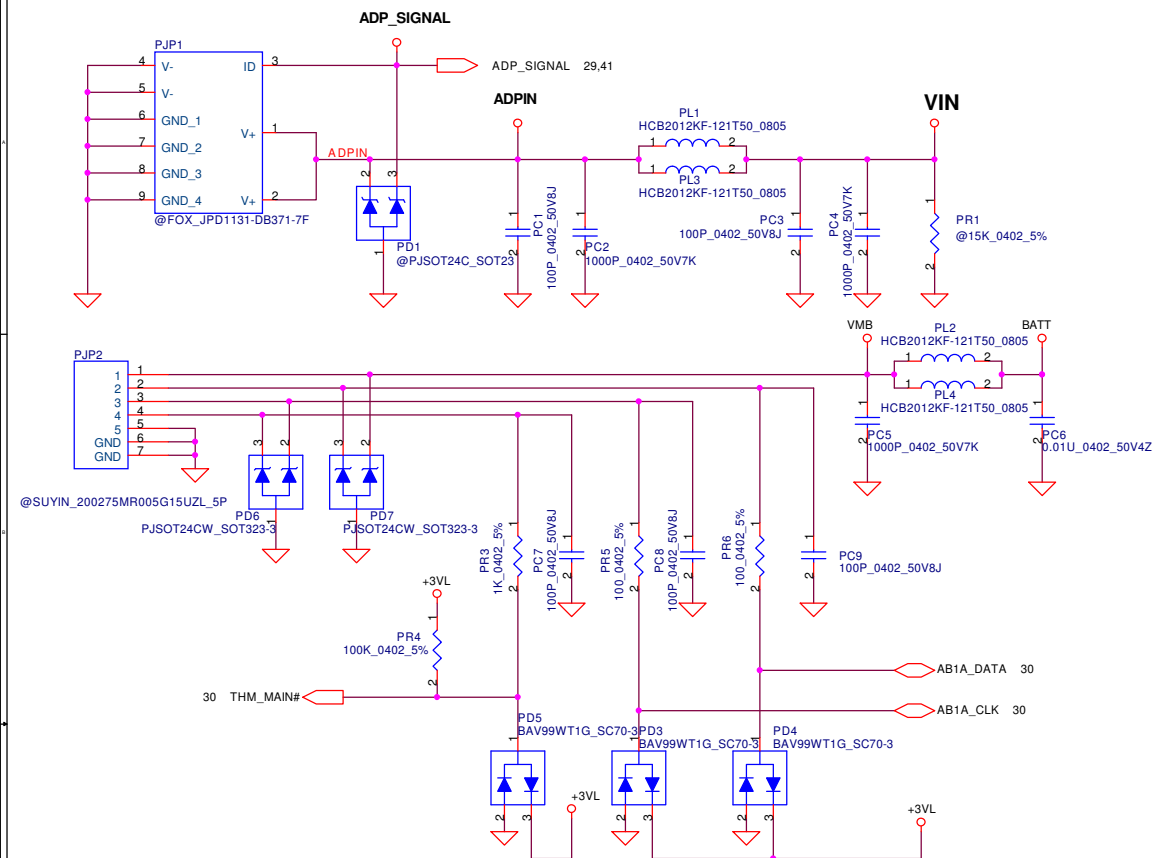


07/10 update for INTEL S3 leakage issue.

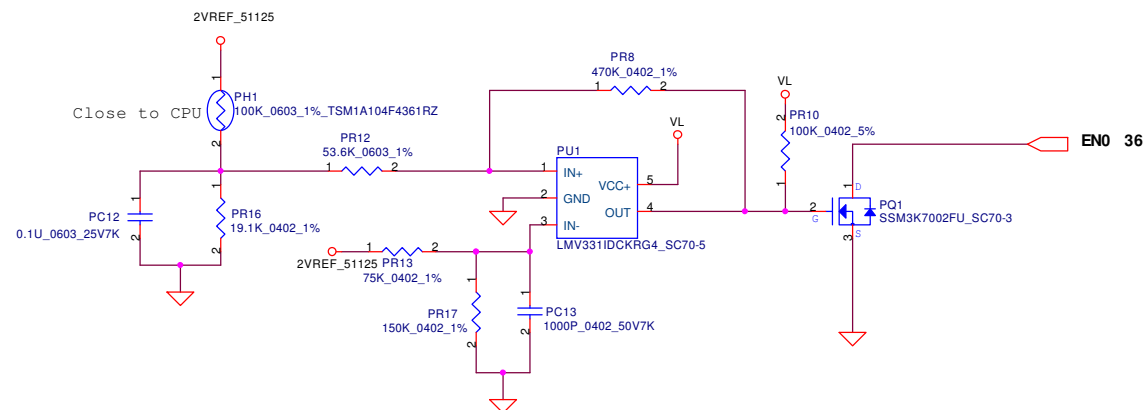
⚙ Add C666,C667,C671 close to JP11.



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/09/15	Deciphered Date	2010/12/31	DC/DC Circuits	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Title	Rev
				Size	0.9
				Document Number	
				LA-5251P	
				Date	Tuesday, January 05, 2010
				Sheet	33 of 47



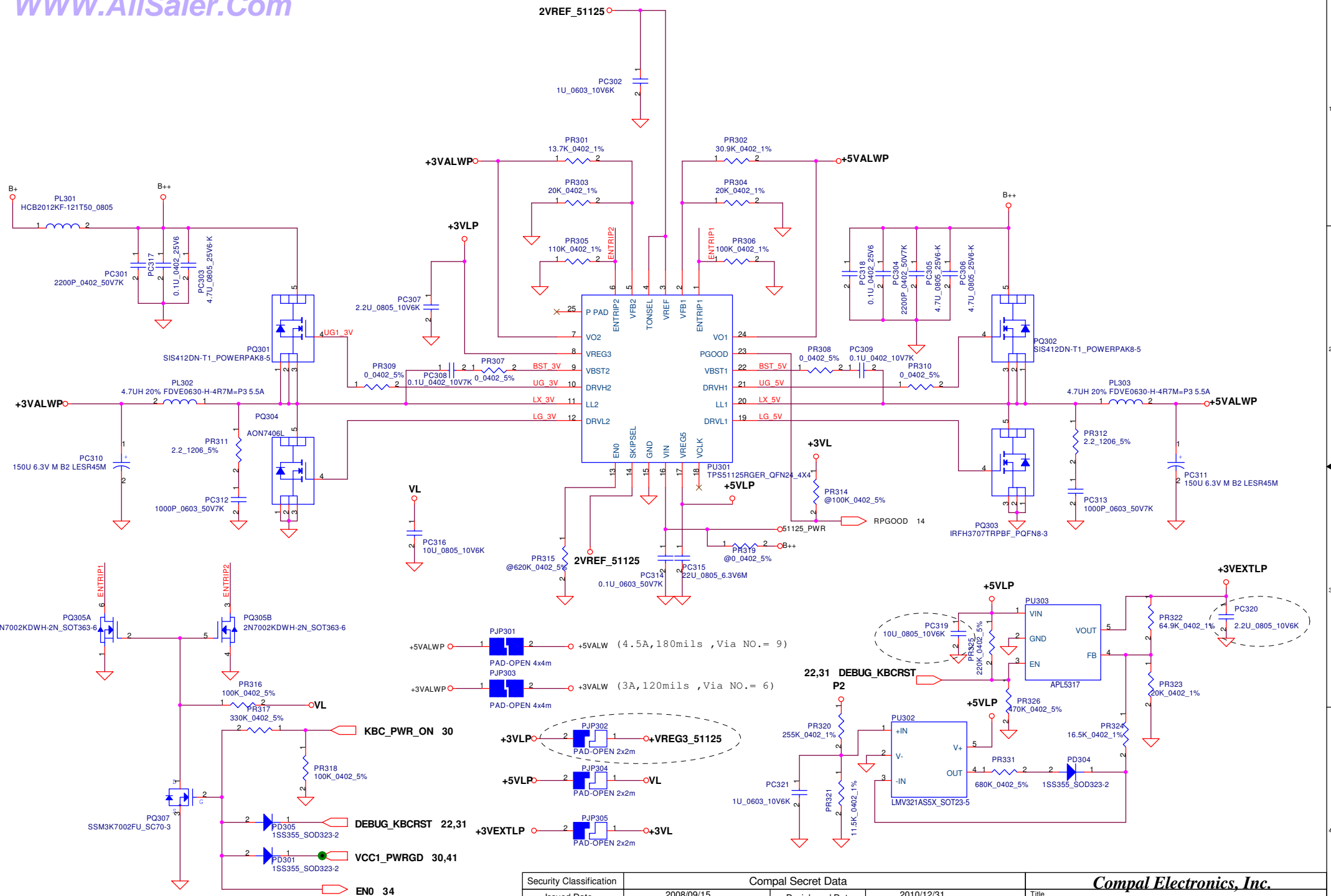
PH1 under CPU botten side :  
CPU thermal protection at 93 +-3 degree C  
(Need to be checked)



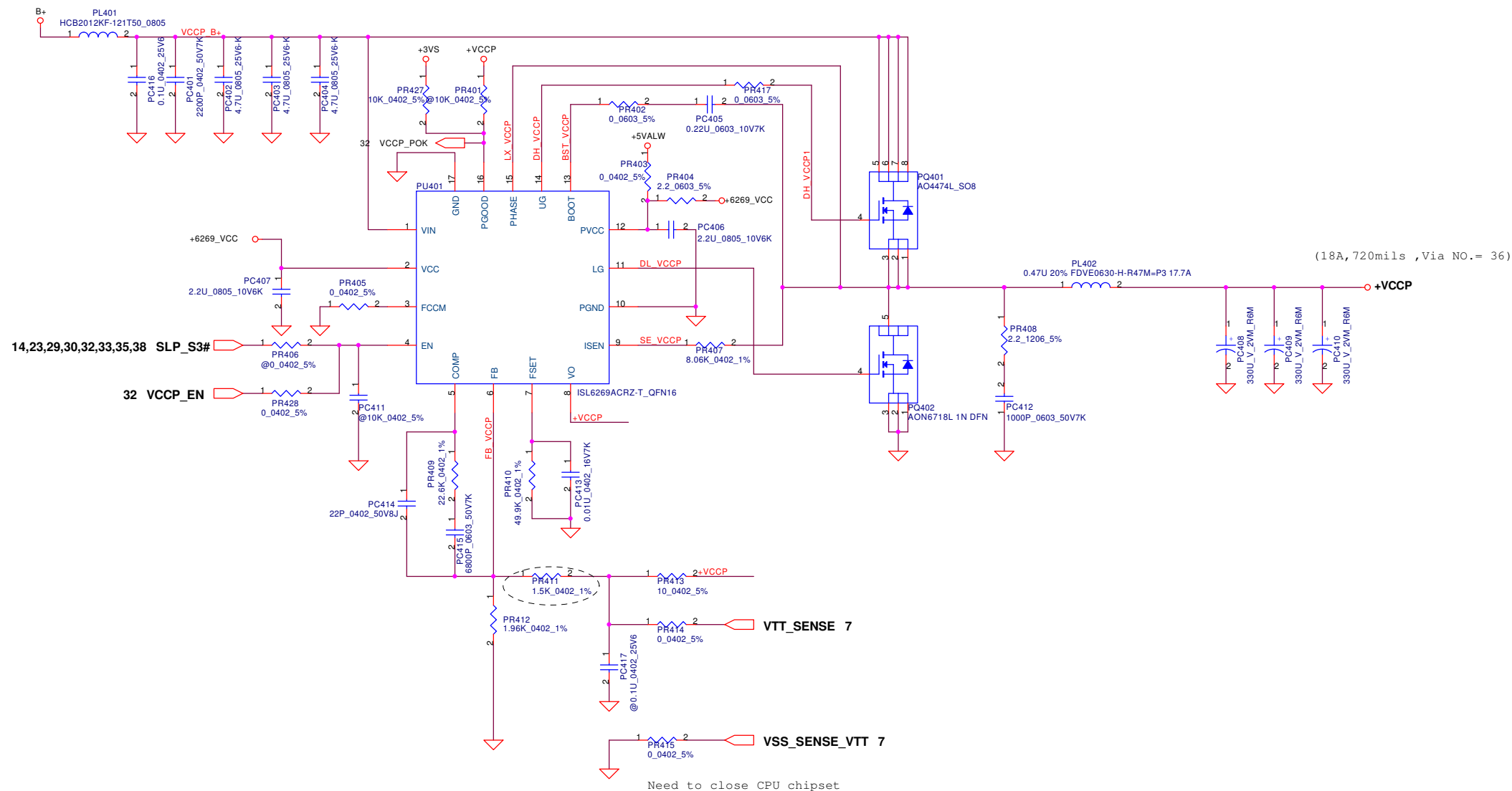
Security Classification			Compal Secret Data		2010/12/31		Compal Electronics, Inc.	
Issued Date			2008/09/15		Deciphered Date		Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS NOT TO BE REPRODUCED, COPIED, OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, WITHOUT THE WRITTEN PERMISSION OF COMPAL ELECTRONICS, INC. ANY VIOLATION OF THIS POLICY WILL BE PROSECUTED TO THE FULL EXTENT OF THE LAW.			Document Number		Rev		Date: Tuesday, January 05, 2010	
LA-4902P			Sheet		34 of 47			



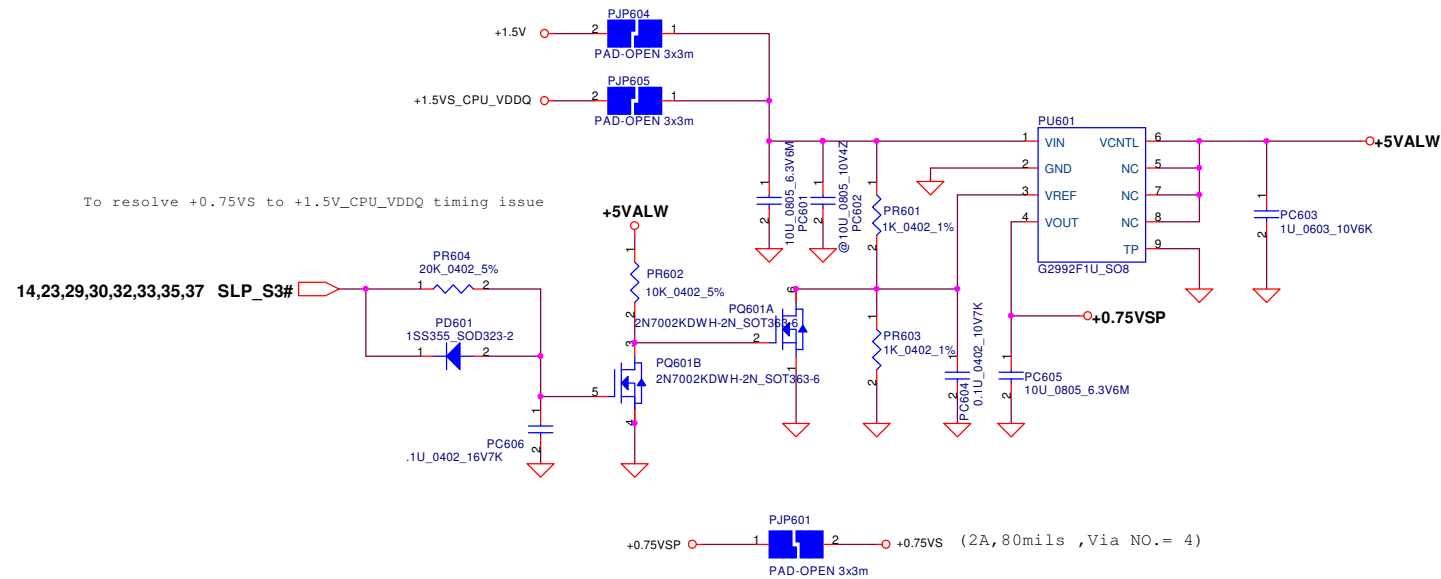
**www.AtiSaler.Com**



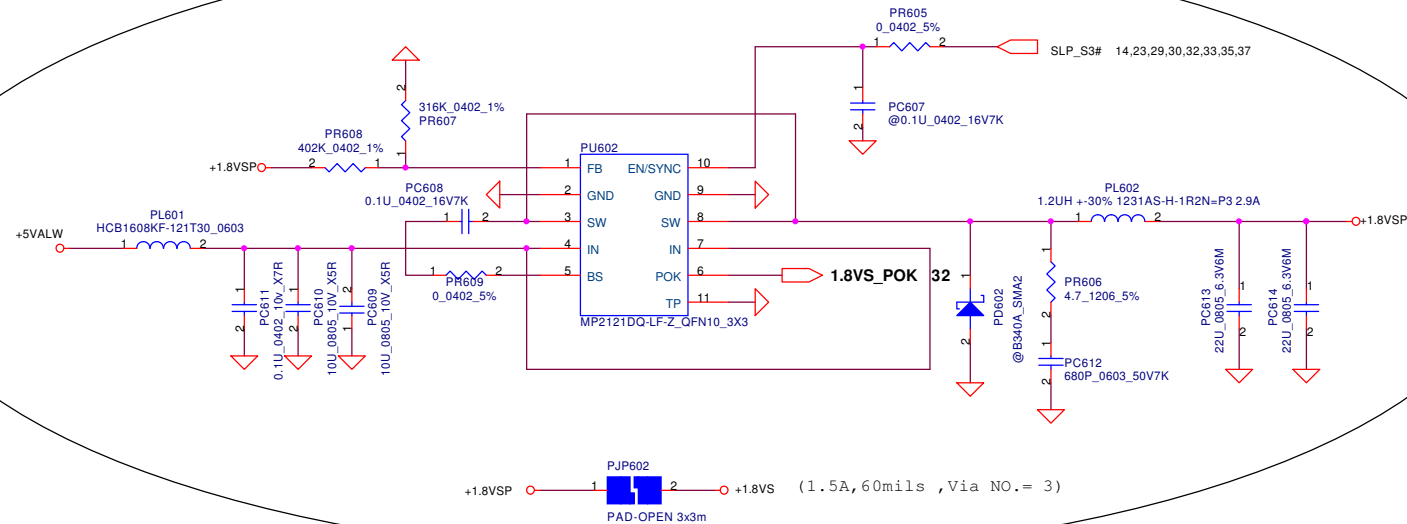
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/09/15	Deciphered Date	2010/12/31	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D TO ANY OTHER DEPARTMENT OR TO ANY OTHER PERSON WITHOUT THE WRITTEN PERMISSION OF COMPAL ELECTRONICS, INC.				3.3VALWP/5VALWP	
Size	Document Number	Rev		0.9	
Custom	LA-4902P	Date:		Tuesday, January 05, 2010	
Sheet		36		of 47	



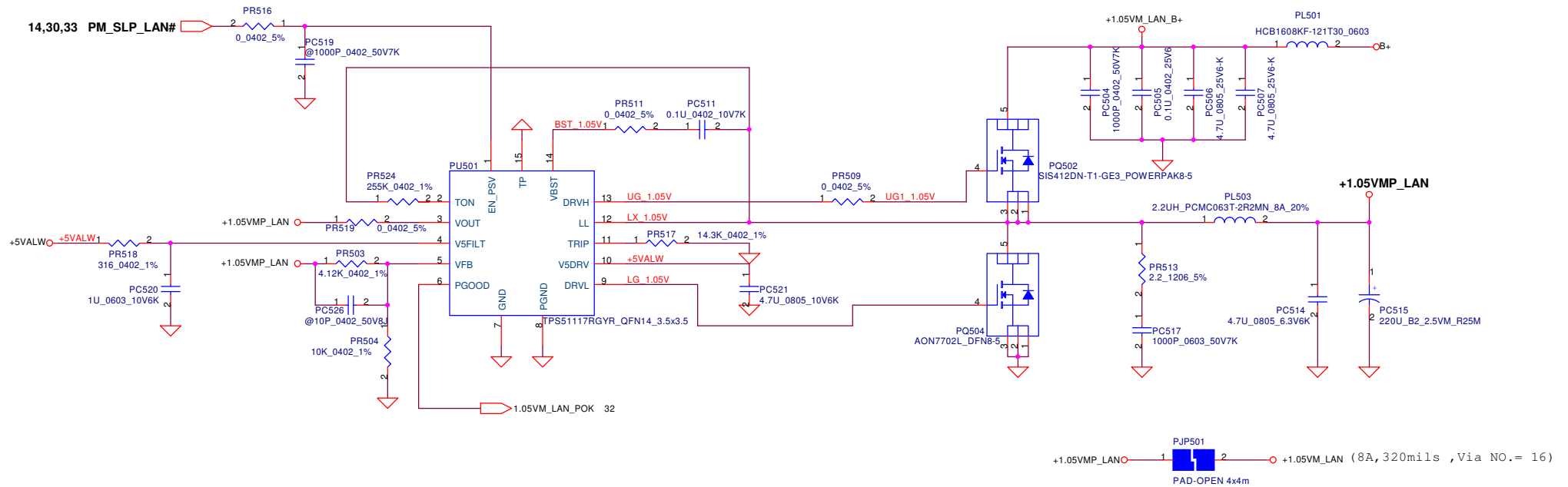
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2008/09/15	Deciphered Date	2010/12/31	Title			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS NOT TO BE REPRODUCED, COPIED, OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, WITHOUT THE PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				1.05V_VCCP			
				Size	Document Number	Rev	
				LA-4902P		0	
Date: Tuesday, January 05, 2010				Sheet	37 of 47		



Change +1.8VS VR

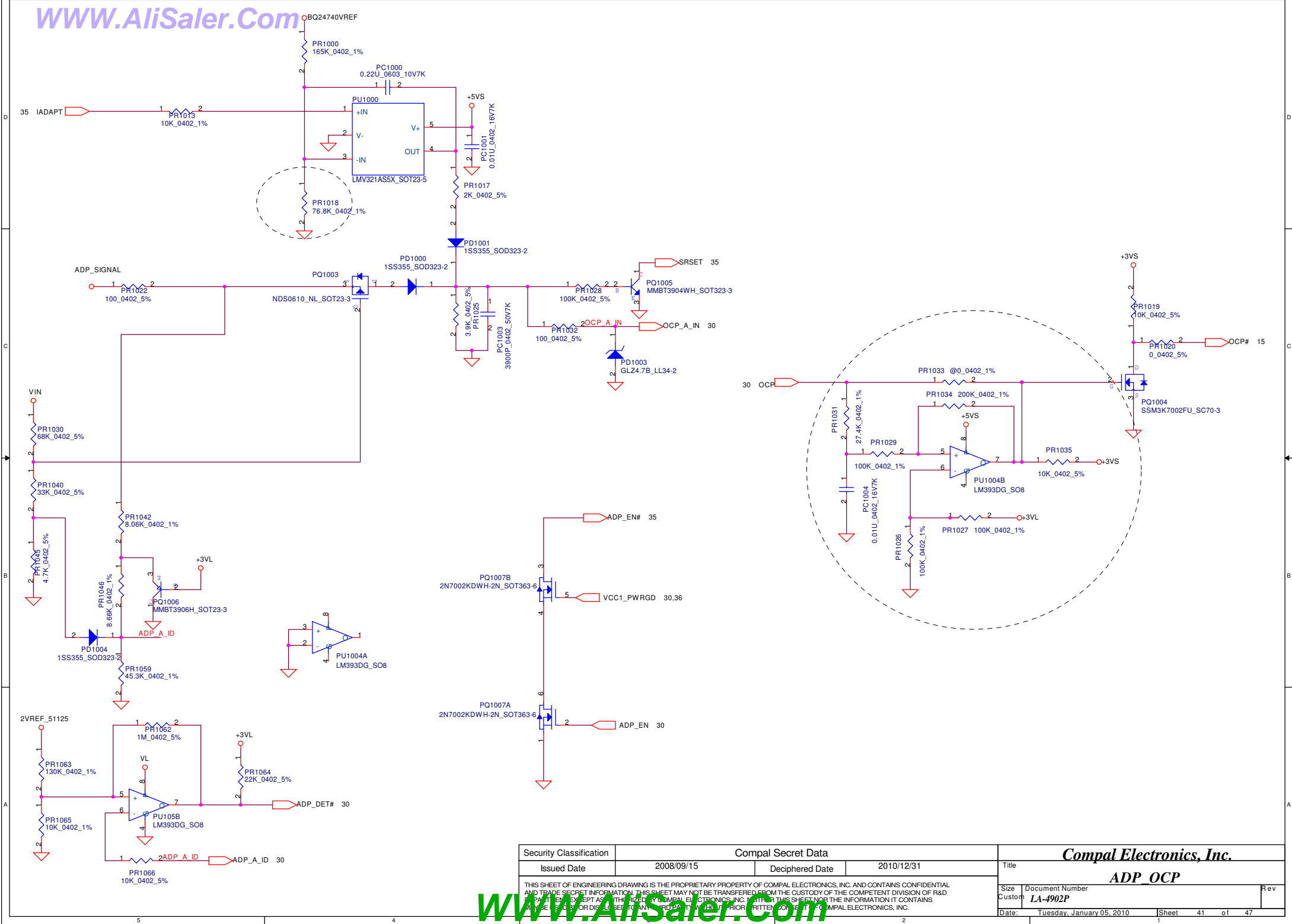


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/09/15	Deciphered Date	2010/12/31	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT MAY NOT BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, WITHOUT THE WRITTEN PERMISSION OF COMPAL ELECTRONICS, INC.				0.75VSP/1.8VSP	
Size	Document Number	Rev		0.9	
LA-4902P		Date:		Tuesday, January 05, 2010	
Sheet		38		of 47	

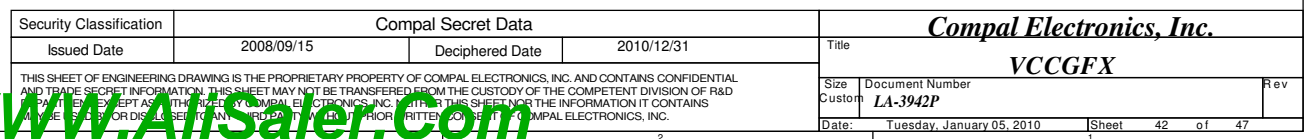


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/09/15	Deciphered Date	2010/12/31	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. IT IS NOT TO BE REPRODUCED, COPIED, OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, WITHOUT THE PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				1.5VP/1.05VMP	
Size	Document Number	Rev		Date	
	LA-4902P	0.9		Tuesday, January 05, 2010	
Sheet		39		of	
		47			





Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/09/15	Deciphered Date	2010/12/31	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. WITHOUT THE WRITTEN PERMISSION OF THE INFORMATION IT CONTAINS. IT IS TO BE USED FOR DESIGN OR MANUFACTURING PURPOSES ONLY. NO OTHER USES ARE PERMITTED WITHOUT THE WRITTEN PERMISSION OF COMPAL ELECTRONICS, INC.				ADP_OCP	
Size	Document Number	Rev		Date: Tuesday, January 05, 2010	
Custom	LA-4902P	Sheet		41 of 47	



Item	Reason for change	PG#	Modify List	Date	Phase
1	For all SMSC1098 platforms, please change the signal "AC_AND_CHG" to "AC_ADP_PRES".	35	To best solve the issue of +15V combo adapter (airline adapter) detect, reserve PR127, Add PR128 76.8K +-1% 0402.	2009/5/4	DB-2
2	This is to keep up with AC adapter table changes made in KBC code.	41	PR1042 change the value from 21K +-1% 0402 to 8.06K +-1% 0402. PR1059 change the value from 24.9K +-1% 0402 to 45.3K +-1% 0402. PR1046 change the value from 4.12K +-1% 0402 to 8.66K +-1% 0402.	2009/6/29	SI-1
3	Change PR604 to 15K to resolve +0.75VS to +1.5V_CPU_VDDQ timing issue seen on Cartier/Dior/Versace.	38	PR604 change the value from 10K to 20K. PD601 add the component 1S8355. PC606 add the component 0.1uF_0402_16V7K.	2009/8/28	SI-2
4	To workaround TPS1125 turn on abnormal issue, need to make sure total caps on +5VL rail is at least 30uF. Currently only have 20.2uF.	36	Add PC316 10U_0805_10V6K PC307 change the value from 10U 6.3V M X5R 0805 to 2.2U 10V K X5R 0805. PC315 change the vlaue from 10U 10V K X5R 0805 H1.25 to 22UF 6.3V M X5R 0805 H1.25.	2009/8/29	SI-2
5	The +1.8VS power rail is very inefficient and want to change to a better solution.	36	Change +1.8VS VR schematic.	2009/9/16	SI-2B
6	For ULV CPU design reserve.	40	Reserve PR229 / 0_0402_5% and PR203 10KB_0603_5%_ERTJ1VR103J	2010/01/04	MV
7					

Item	Fixed Issue and change item	PAGE	Modify List	M.B. Ver.
<2009.01.12>	1 Reduce un-install parts for XDP-CPU	4	Del R4, R6, R8, R11, R40, R41, R43, R48, R49	0.1
	2 Add test points at XDP-CPU	4	Add T112, T113	0.1
	3 Reduce eDP lane to meet panel resolution.	5	Reduce lane1, 2	0.1
	4 Add 1uf Caps to meet Intel design gude at +VCAP0, +VCAP1	7	add Caps account to 12pcs	0.1
	5 Add 1uf Caps to meet Intel design gude at +Vccp	8	add Caps account to 24pcs	0.1
	6 Add L31 at +VTT_DDR	7	add L31	0.1
	7 Add L32 at +VDDQ_CK	7	add L32	0.1
	8 Change R171 net name at XDP-PCH	12	Change USB_OC#6 to PCH_XDP_GPIO10	0.1
	9 Add R190 at XDP-PCH	12	add R190 & USB_OC#4	0.1
	10 Change pull up for Intel Design Guide	13	change pull up to contact to R206 pin1	0.1
	11 Remove LVDS for HP request	14	Remove LVDS-A channel	0.1
	12 change value for HP request	15	change R270, R274 value to 39ohm	0.1
	13 Add Resistors for XDP-PCH	15	Add R351, R265	0.1
	14 Change R295 net name at XDP-PCH	15	Change USB_OC#7 to WOW#	0.1
	15 Change value	25	Change R451 tolerance to 1% and C441 tolerance	0.1
	16 Change value	25	Change C428 value to 1000P	0.1
<2009.01.14>	1 Remove E-SATA for HP request	12 24	Remove SATA-2 channel Remove E-SATA support circuit	0.1
	2 Change USB group for HP request	15	Change USB-1 from Right side to Rear-1 side	0.1
	3 Modify Audio circuit	26 27	Add FET and support circuit for SENSE. Change Audio jack	0.1
	4 Add 4.7Kohm pullup to +3V and a 0.01uF capacitor at HDA_RST#	26	Add R703, C637	0.1
	5 Change Audio Gain dB	26	R486 & R491 install ; R485 & R492 un-install.	0.1
<2009.01.15>	1 Delete channel-C signals of DP	14	Delete channel-C signals of DP	0.1
	2 Change power USB control method	24	change Power USB solution to one chip control solution	0.1
	3 change Audio Dock Line in / out sense circuit	26	change R510, R515 value to 100k and R510, R515 pin1 contact to A-GND	0.1
	4 Add Ext-Mic Amp.	27	Add Ext-Mic Amp.	0.1
<2009.01.16>	1 Change XDP-CPU net	4	JP4 [28,30] connect to CFG [10:11]. JP4 [34,36] connect to CFG [6:7].	0.1
	2 Change eDP_AUXN contact to CPU pin	5	MB_C_DP_AUXN should connect to U1A.D19.	0.1
	3 Remove CFG7 (No support)	5	delete R71.	0.1
	4 Add pull up for HP request	7	Add 10K (R705) NI pull-up to +VCCP on GFXVR_EN.	0.1
	5 GFX_CORE needs high frequency decoupling.	7	Add 16x0402 1uF caps.	0.1
	6 VTT pins contact wrong power source	7	Change VTT pin to +VCCP	0.1
	7 CPU_CORE missing high frequency decoupling.	7	Add 25x0402 1uF caps.	0.1
	8 Change LAN power source control method	21	C330 - C333, C329, R383, R386, Q21uninstall and change "LAN_CTRL_18" to "LAN_CTRL_10"	0.1
	9 Add USBP6 for support WiMax.	22 15	Add USB channel 6	0.1

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/02/13	Deciphered Date	2010/12/31	Title	HW PIR(1)
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. NO PART OF THIS SHEET MAY BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, WITHOUT PERMISSION IN WRITING FROM COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	LA-525IP
				Date:	Tuesday, January 05, 2010
				Sheet	44 of 47
				Rev	0.9

Rev.	Item	Date	Impact	Page	Change Cause	Modify Description
0.3	1	6/12	CKT,Layout	29	-To avoid Docking side DP monitor signals back drive PCH during S3/S4/S5 <HP>.	-Change JP30 Pin 8 connection from NC to SLP_S3#
0.3	2	6/12	CKT,Layout	29	-New add SATA_LED# to monitor stand port <HP>.	-Change JP30 Pin 39 connection from NC to SATA_LED#
0.3	3	6/14	CKT,BOM,Layout	18,29	-Change CRT Switch design from TI/TS5A3157 to MAXIM/MAX4885E for Layout Quality improve also Components reducing. <Compal> -Correct the DP design. <HP>	-Add U13,R319 (10K_0402);Remove and Del C550,C551,C552,Q12,U11,U12,U29,U30,U31,R320,R321,R327,R328,R329,R330;Del D5,D6,D7.
0.3	4	6/16	BOM	19		-Make R338 & R344 no install. Make R332 & R337 installed.
0.3	5	6/16	CKT,Layout	23	-Current placement of C933 is ineffective to limit inrush current. <HP>	-Change net connection and move C933 to in between R1079.2 and R1077.1.
0.3	6	6/16	CKT,Layout	13	-Add back the 25MHz XTAL_IN circuit for Intel workaround on sighting #400750 - 3306048 - 96MHz jitter.<HP> -Audio Amp Int. regulator design concern. <HP>	-Reserve back the 25MHz design circuit. (Reserve Y3, R210,C199); Move R1093 to close to Y3 and C199.
0.3	7	6/16	CKT,BOM,Layout	26		-Add R490 (100K_0402) close to U24.25 to connect U24.25 and PLT_RST#.
0.3	8	6/16	CKT,BOM,Layout	15,20	-To leverage the LDO regulator of the camera modules. <HP>	-1.Change R365 from 0_0201 to 0_0402. Change R569,R613 from 100K_0201 to 100K_0402.Change R377 from 100K_0201_1% to 100K_0402_1%. 2.Rename WEBCAM_OFF to WEBCAM_ON and connect PCH GPIO37(U7.AB13) through WEBCAM_ON_R by R375(0_0402) to JEDP1.18. 3.Connect +5VS_WEBCAM to +5VS through R304 (0_0603) close to JEDP1.24 and move C316~C319 close to JEDP1.24. Del Q17,C315,C321,R360-R362,R367,R373. 4.Change U7.AB13 and R287.1 connection from PCH_XDP_GPIO37 to WEBCAM_ON. Change R287 from 10K_0201 to @10K_0402(uninstall). 5.Change U7.F16 connection from WEBCAM_OFF to USB_OC#2 and add pull-high R301(10K_0201) to +3VALW.
0.3	9	6/17	CKT,Layout	28	-Correct the TouchPoint pin connection.<Compal>	-Correct JP27 connection from currently Pin1:+5VS,Pin2:RIGHT,Pin7:GND,Pin8:GND to Pin1:RIGHT,Pin2:NC,Pin7:NC,Pin8:+5VS.
0.3	10	6/18	CKT,Layout	16	-Simplify the reserve circuit. <HP>	-Del C277(@10U_0603). Move C276 and related routing to bottom layer 0 mm limit high area without vias.
0.3	11	6/18	CKT,Layout	30	-Design Change for KBC I/F power rail synchronize.<HP>	-Change U8.5 power from +3VALW to +3VL.
0.3	12	6/18	CKT,BOM,Layout	24	-Add common mode chokes on all USB walk-up ports to address PCH EMI issue on full/low speed USB devices. <HP/INTEL>	-Change JP13,JP14,D18,D19,D20 USB pairs net connection and add or reserve R352,R350,R354,R353,R360,R355,L8,L9,L19,L26. Change R443,R444 from 0201 to 0402 and also the net connection.
0.3	13	6/18	CKT,BOM,Layout	30	-Design Change for KBC I/F power rail synchronize.<HP>	-Change U8.5 power from +3VALW to +3VL.
0.3	14	6/18	CKT,BOM,Layout	19	-Add fuse (0.5A) for DP Safty solution.<Compal>	-Add F2(FUSE) between R349.2 and JDP1.20 for Safty solution.
0.3	15	6/22	CKT,Layout	16	-Layout Placement Limitation. <Compal>	-Del C277(@10U_0603) and C276, add the test points T126,T127 for the ball pins.
0.3	16	6/25	CKT,Layout	22	-Change 1.8"HDD design from cable to Board to Board connection.<HP>	-Del JHDD1 and JHDD2 Cable design. Add JHDD3 B to B directly connect design.
0.3	17	7/1	CKT,Layout	25	-Need to add ESD protection to SC_DATA, SC_RST, & SC_CLK.<HP>	-Reserve D54,D55,D56 ESD protection design as what Ricoh recommend.
0.3	18	7/1	CKT,BOM,Layout	11	-Reserve Low Power CLK_Gen design.<Compal>	
0.3	19	7/1	CKT,BOM,Layout	12,20	-Make the LID_SW# design change for leakage issue fix.<HP>	-Modify U6 Pin1,17,24 connection from +3VS_CK505 to +3VS_CK505_G (+3VS and +1.5VS option for tuture); Add R143(0ohm_0603) to +3VS and reserve R120(0ohm_0603) to +1.5VS but place close to U6.
0.3	20	7/1	CKT,BOM,Layout	13	-Fix INTEL Chipset Issue impact DP function. <HP/INTEL>	-Change Q56.5 from DISP_OFF# to LID_SW#; Del D10(DAP202U); Add R361(10K_0402) close to U7; Add D57(CH751H); Remove R356(10K_0402);Change U7.J30 and R135.2 connection from LID_SW# to LID_SW#_ISO#.
0.3	21	7/1	CKT,BOM,Layout	13,21	-Follow INTEL Design Change. <HP/INTEL>	-Del T122, Del R1093(0_0402) and replace by add C200 (18P); Install R210,Y3,C199 by Intel finalized DP workaround and need them.
0.3	22	7/1	CKT,BOM,Layout	30	-Follow SMsC KBC Chip Design Change and VCC1 decoupling improve. <HP/SMsC>	-Remove R388 (0_0201); Connect U14.48 through add R407 (0_0402) to U7.U4 (R202.2) by INTEL request.
0.3	23	7/1	CKT,BOM,Layout	30,14,22	-Design simplify on both EE and PWR from HP. <HP>	-Add C565 (0.1U_0402) on and close to U32.14 for VCC1 decoupling improve by SMsC request; Change C559 from 4.7UF_Y5V to 4.7UF_X5R.
0.3	24	7/1	CKT,BOM,Layout	33	-Add +VCCP and +GFX_CORE discharge circuit. <HP>	-Del D37(@CH751H) and related. Remove R246,R422,and delete PR217.
0.3	25	7/1	CKT,BOM,Layout	22	-Half size mini card I/F transfer design reserve for future. <Compal>	-Add 1K VGATE to PGD_IN resistor at PCH pin M6. Connect PGD_IN through add R408 (1Kohm_0402) to PCH.U7.M6.
0.3	26	7/1	CKT,Layout	22		-Add R699,R702,Q41 for +VCCP and +GFX_CORE discharge
0.3	27	7/2	CKT,BOM	15		-Del T87, Add R475 (0_0201) and R453 (0_0402); Reserve R433,R437,R432,R421,R431,R441 close to JP6 bottom layer under the module area for reworkable.
0.3	28	7/2	CKT,BOM,Layout	23		-Update JODD1 PCB Footprint from ALLTO_C18522-11303-L_13P_NR to TYCO_2023233-3_13P_NR
0.3	29	7/2	CKT,Layout	15		-Change R279 from 10K_0201 to 100K_0201.
0.3	30	7/2	CKT,BOM,Layout	12		-Change R1077.1,C933.1,Q77.3,J3.2 connection from +3VS to +3VALW for WWAN power rail. Install C933(1000P_0402) in order to slow +3V_WWAN bring-up
0.3	31	7/2	CKT,BOM	30		-LAN_DIS# R298 should be pulled-up to +3VM_LAN instead of +3VALW.
0.3	32	7/2	CKT,BOM	30		-Delete R135 since it is a duplicate. Change R361 to 100K_5%. Add 100K_5% pull-up to +3VL on LID_SW# and close to U32.64.
0.3	33	7/2	CKT,Layout	31		-For SI-1 Board ID detect, make R574 installed & make R575 no install.
0.3	34	7/2	CKT,BOM	31		-Remove R589 on KBRST# pull-high to +3VL. Change R607 on PM_RSMRST# from 10K to 100K to reduce current.
0.3	35	7/2	CKT,Layout	28		-Change the ESD diode (D39.4) power supply from +3VALW to +5VALW.
0.3	36	7/3	CKT,Layout	23		-Remove R626 (0_0201) since there is an internal pull-down in U34.
0.3	37	7/3	CKT,BOM,Layout	12,13		-Reserve C536(1000P_0402) Cap on STB_LED# close to JP22.8 for EMI noise issue verify.
0.3	38	7/3	CKT,Layout	20		-Connect U17 pin 12 and 14;pin2 and pin4;pin11 and 13;pin3 and 5 for express card portload test.
0.3	39	7/3	CKT,BOM,Layout	30		-Change U7.J30 connection from LID_SW#_ISO# to T122. Change U7.B9 connection from SMBALERT# to LID_SW#_ISO#. Del R193 (10K_0201) +3VALW PH.
						-Change JEDP1 pin6 connection from +3VS to INV PWR_B+.
						-Del R594 (220_0402) (PM_PWROK)

Security Classification

Compal Secret Data

Issued Date

2006/02/13

Deciphered Date

2010/12/31

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE REPRODUCED, COPIED, OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT THE WRITTEN PERMISSION OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

H/W2 EE Dept. PIR SHEET(2)

Size Document Number

LA-5251P

Rev

0.9

Date: Tuesday, January 05, 2010

Sheet 45 of 47

WWW.AliSaei.Com

**KAT10 from SI1 to SI1-R LA-5251P REV:0.3 -> 0.4 Modify <2009.07.07.~2009.07.14. >**

Rev.	Item	Date	Impact	Page	Change Cause	Modify Description
0.4	1	7/8	CKT,BOM,Layout	32	-To fix INTEL CPL S3 Power Leakage Issue <INTEL>.	--Update U38 Symbol. Add one new signal "VCCP_1.5VSPWRGD" be generated from VCCP_EN through an new add AND gate U77 to R12.2.
0.4	2	7/8	CKT,BOM,Layout	4,15	-To fix INTEL CPL S3 Power Leakage Issue <INTEL>.	--Change R12.2 connection from +1.5V to VCCP_1.5VSPWRGD. Change R12 from 1.1K_0402_1% to 4.99K_0402_1%; Change R13 from 3K_0402_1% to 2.49K_0402_1%. Change U1.BJ12 connection from DRAMRST# to SM_DRAMRST# by add Q52 which control by PCH_DDR_RST new connect from U7.F10 (PCH GPIO8)(GPIO8-->PCH_DDR_RST) and with add R1093 (1K_0402) PH to +1.5V, add R1092 from @10K_0402 to 100K_0402.
0.4	3	7/8	CKT,BOM,Layout	33	-To fix INTEL CPL S3 Power Leakage Issue <INTEL>.	--Add new Power from +1.5V to +1.5VS_CPU_VDDQ by add U45,C624,C625,R1104 close to C152; Add +1.5VS_CPU_VDDQ discharge circuit by add R1103(470_0402) and Q52B (already exist) close to U45.
0.4	4	7/8	CKT,BOM,Layout	7,10	-To fix INTEL CPL S3 Power Leakage Issue <INTEL>.	--Change U1 VDDQ Power source from +1.5V to +1.5VS_CPU_VDDQ but keep C20~C27 at the same place; Del C145,C146,C119,C120 10UF_0603 reserve for U45 and related placement.
0.4	5	7/9	CKT,BOM,Layout	32	-To fix INTEL CPL S3 Power Leakage Issue <INTEL>.	--Change U77.1 connection from VCCP_EN to SLP_S3# reserve through R6(@_0402) or to +3VALW through R4 (8.2K_0402).
0.4	6	7/9	CKT,BOM	33	-To fix INTEL CPL S3 Power Leakage Issue <INTEL>.	--Install R693 (470_0201) and Q53 (2N7002).
0.4	7	7/9	CKT,BOM,Layout	4,5	-To fix INTEL CPL S3 Power Leakage Issue <INTEL>.	--Change R1092 PD connection from PCH_DDR_RST to SM_DRAMRST# and close to U1.BJ12. Add C6 (470P_0402) close to Q52.2.
0.4	8	7/10	CKT,Layout	7	-To fix INTEL CPL S3 Power Leakage Issue <INTEL>.	--Change L32.2 connection from +1.5V to +1.5VS_CPU_VDDQ.
0.4	9	7/10	CKT,BOM,Layout	33	-To fix INTEL CPL S3 Power Leakage Issue <INTEL>.	--Add C626,C664 close to JD1MA1;C656,C657 close to JD1MB1.
0.4	10	7/17	CKT,BOM	4	-To meet Intel electrical requirements <INTEL>.	--Change back R12 from 4.99K_0402_1% to 1.5K_0402_1%; R13 from 2.49K_0402_1% to 750_0402_1%.
0.4	11	7/17	CKT,BOM,Layout	33	-To meet Intel ramp down timing for 1.5V and 0.75VS <INTEL>.	--Change R1103 from 470_0402 to 220_0402; R693 from 470_0201 to 22_0402.
0.4	12	7/17	CKT,BOM	33	-To fix INTEL CPL S3 Power Leakage Issue <INTEL>.	--Remove R1092 (100K_0402).
0.4	13	7/17	CKT,BOM,Layout	33	-Toto avoid a glitch while turning on +1.5V_CPU_VDDQ <HP>	--Add C505 (@0.01UF_0402) close to U45.4.
0.4	14	7/17	CKT,BOM	24	-Correct BOM <Compal>	--Change U18 and U20 from SA000027C00 (G548A2P8U MSOP) to SA00002WY00 (G548A1P8U MSOP) for BOM correct.
0.4	15	7/22	CKT,BOM,Layout	28,30	-Design change ON/OFF# control from PCH directly become through EC. <HP> -KBC will block the PWRBTN# and hold PWRBTN_OUT# HIGH when it receives a command from the BIOS indicating BOOT BLOCK reprogramming is in progress.>	--Disconnect LANLINK_R# from KBC (GPIO24/KSO16) by through R608(@0_0402) reserve; Rename GPIO24 of KBC to PWRBTN_OUT#; Install R550 (Change R550 from 100K_0201 to 100K_0402); Disconnect the PWRBTN# output from the button switch to the PCH by remove D34; Connect ON/OFFBTN# from KBC GPIO24 to the PCH let KBC can now control the PWRBTN#.
0.4	16	7/22	CKT,BOM,Layout	30	-Design reserve for thermal fan table switch for SV/LV CPU type detect. <Compal>	--Reserve CPU_SV_ID_DET with R551(@100K_0402)PH and R553(@100K_0402)PD.
0.4	17	7/22	CKT,Layout	15	-Design reserve for thermal fan table switch for SV/LV CPU type detect. <Compal>	--Add R302(@10K_0201) PD close to R280 on PCH GPIO15.
0.4	18	7/24	CKT,BOM	26	-Increases attenuation of PC beep to an acceptable loudness level. <HP>	--Change R484 from 100K_0201 to 300K_0201.
0.4	19	7/24	CKT,BOM	26	-Increases line in attenuation from -6dB to -10dB. <HP>	--Change R502, R504 from 4.7K_0402_5% to 6.04K_0402_1% & R503, R505 from 4.7K_0402_5% to 2K_0402_5%.
0.4	20	7/24	CKT,BOM	36	-Per TI's recommendation for 3VLP. <TI>	--Change PC307 from 10U_0805_6.3V6M to 2.2U_0805_10V6K.

**KAT10 from SI1-R to SI2 LA-5251P REV:0.4 -> 0.5 Modify <2009.08.11.~2009.08.28. >**

Rev.	Item	Date	Impact	Page	Change Cause	Modify Description
0.5	1	8/18	CKT,Layout	32	-To avoid the thermal module Assy. risk. <Compal DFx>.	--Add back H31 and make the DDR routing modify for this.
0.5	2	8/25	CKT,Layout	20	-To disconnect LID_SW#_ISO# from LID_SW# function. <HP>.	--Reserve R366 (@0_0402 ohm NI) resistor between Q56-1 and R361-2.
0.5	3	8/25	CKT,Layout	28	-To fix false CBB button triggering on AC insertion due to noise seen on +3VL power rail. <HP>.	--Change JP28-1 from +3VL to +VREG3_51125 power rail.
0.5	4	8/25	CKT,BOM,Layout	14,31	-Disconnect LPC_PD# from TPM U34. <HP/Intel/Infineon>.	--Change U7.P8 connection from LPC_PD# to SUS_STAT# as NC with only T87 test pad only. Add R367 4.7K_0402 with PH +3VS on U34.28.
0.5	5	8/25	CKT,BOM,Layout	15,23	-Rename WOW# (U7F-T15) to CPPE# and connect to JEXP1-17 & U17-10. <HP>.	--Change U7.T15 GPIO14 connection through R265(0_0402) from WOW# as NC to CPPE# which connect to ExpressCard JEXP1-17 & U17-10.
0.5	6	8/25	CKT,BOM	26	-Correct the Audio Amp. Gain setting. <Compal>.	--Remove R485 (0_0201).
0.5	7	8/28	CKT,BOM	4	-Prevent glitch on DRAMRST#. <HP>.	--Change C6 from 470P to .1U_0402.
0.5	8	8/28	CKT,BOM,Layout	26	-Change audio REG_EN pin to +5VALW to prevent pop sound on warm boot. <HP>.	--Change R490.2 connection from PLT_RST# to +5VALW.
0.5	9	8/28	CKT,BOM	12	-Remove PCH Debug Port related to save power consumption. <Compal>.	--Remove R158,R156,R167,R165.
0.5	10	8/28	CKT,BOM,Layout	29	-Cancelled Docking +5VS Caps design reserve before for design simplify. <Compals>.	--Del C543 (10U_0805), C544~C546 (0.1U_0402).
0.5	11	8/28	CKT,Layout	32	-Cancel Skew Hole because of M/E PCB outline change. <Compal>.	--Del H27 (H_3P0).
0.5	12	8/28	CKT,BOM,Layout	19	-Cancel Swatch system side Display Port Common Mode Choke reserve for design simplify and layout space free. <Compal>.	--Del L12~L16(@WCM-2012-900T_4P),R331,R333,R334,R335,R336,R339,R340,R341,R345,R347(0_0402) and related Net.
0.5	13	8/28	CKT,Layout	18	-Reserve 10PF caps on VGA_RED_R, VGA_GRN_R, VGA_BLUE_R for EMI backup solution. <Compal>.	--Reserve C315,C320,C321(@10P_0402) close to R316,R317,R318.
0.5	14	8/28	CKT,BOM	23	-Cancel Braidwood support but keep design reserve. <HP>.	--Remove R567,R562,C571,C566,JP11.
0.5	15	8/31	CKT,BOM,Layout	12	-Add back PCH GPIO13 Ext. Pull-High to +3VALW. <HP>.	--Change U7.J30 connection from T122 to become PCH_GPIO13 and pull-high to +3VLAW through R8(10K_0402).
0.5	16	9/01	CKT,BOM,Layout	28	-WW_LED# Design change for fix WWAN Module LED issue. <HP/Compal>.	--Del Q33,Q35,R542 Change R1097,R1098,R1099 value and connection.
0.5	17	9/01	CKT,BOM,Layout	24	-Stakup USB Connector update for Compal DFb review. <Compal>.	--Change JP13 PCB Footprint from SUYIN_020122MR008S51CZL_8P to SUYIN_020122GR008S51CZL_8P-T.
0.5	18	9/03	CKT,BOM	15	-Cancel Braidwood support but keep design reserve. <HP>.	--Remove R257 (@32.4_0402_1%).
0.5	19	9/03	CKT,BOM	23	-To resolve slow turn off of +3V_WWAN. <HP>.	--Install R1077 (10K_0402_5%).
0.5	20	9/03	CKT,BOM	26	-To fix EQ setting make the changes. <HP>.	--Remove R491 (@100K_0201) ; Add R485,R486 (0_0201_5%).
0.5	21	9/10	CKT,BOM	-	-To correct the symbol inside information to make value match with SMT BOM for long-term. <Compal>.	--Change U8 from SA000023O00 to SA00003FF00; Q13 Q14 Q15 Q16 Q29 Q30 Q31 Q32 Q36 Q40 Q41 Q43 Q44 Q45 Q46 Q47 Q48 Q49 Q50 Q51 Q52 Q56 from SB570025280 to SB00000AR10; U17 from SA00001SL00 to SA00001SL20; U18,U20 from SA00002WY00 to SA000037P00; Q19, Q22, Q23, Q26, Q38, Q39 from SB923010030 to SB00000H500; U14 from SA00002MO10 to SA00002MO40; U6 from SA00002WX00 to SA00003NM00; U2 from SA000021J00 to SA00002ZT00; Change U46 from SA097010020 to SA097010040; Correct L31 Value from TDK-MPZ140BS300A 0603 to 0_0603_5% for match; Correct L32 Value from 1UH_SQV322520T-1R0M-N_20% to 0_0603_5% for match; Install R551 (100K_0402) as default setting; Remove R143(@0_0603) and add R120(0_0603) for LP CLK Gen. power as default setting; Remove &U1 for SMT BOM Match
0.5	22	9/11	CKT,BOM	23	-To reduce power consumption. <HP>.	--Remove R1077 (@10K_0402)

Security Classification		Compal Secret Data		<div>Compal Electronics, Inc.</div> <div>H/W2 EE Dept. PIR SHEET(2)</div>	
Issued Date	2006/02/13	Deciphered Date	2010/12/31		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. THIS SHEET MAY NOT BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, WITHOUT PERMISSION IN WRITING FROM THE CUSTOMER DIVISION OF R&D DEPARTMENT OF COMPAL ELECTRONICS, INC. ANY VIOLATION OF THIS SHEET OR THE INFORMATION IT CONTAINS MAY BE SUBJECT TO LEGAL ACTION AND PENALTY WITHOUT PREJUDICE TO THE INTELLECTUAL PROPERTY OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number LA-5251P
				Date	Rev
				Tuesday, January 05, 2010	0.9
				Sheet 46 of 47	

**KAT10 from SI2 to SI2-R LA-5251P REV:0.5 -> 0.6 Modify <2009.09.11.~2009.09.29. >**

Rev.	Item	Date	Impact	Page	Change Cause	Modify Description
0.6	1	9/21	CKT,BOM,Layout	11,24	-To fix BT turn off time (>250mS spec) <HP>.	--Change CLK Gen CK_PWRGD from Q7(2N7002_SOT23-3) to Q55(2N7002DWH 2N SOT363-6); Add Q55B 2N7002 discharge FET on +3VAUX_BT; Add R135 (470_0402) series resistor between drain of FET and +3VAUX_BT. Reserve C506 (@0.1uF_0402) for tune.
0.6	2	9/22	CKT,BOM	7	-Move +GFX_CORE Bulk Caps from Power related to EE related. <Compal>.	--Change PC713,PC714 location name to C973,C974.
0.6	3	9/28	CKT,Layout	20	-To prevent inrush current problem seen on some panels. <HP>.	--Reserve Q28(SI2301),C975,C976,R1105,R1106 close to JEDP1.
0.6	4	9/28	CKT,Layout	20	-To reserve the EMI solution for verify. <Compal-EMC>.	--Reserve Reserve R372,C665 close to JEDP1.
0.6	5	10/01	CKT,BOM	21	-To fix crystal frequency stability risk. <INTEL>.	--Change C341 and C342 from 27P_0402 to 33P_0402.

**KAT10 from SI2-R to PV LA-5251P REV:0.6 -> 0.7 Modify <2009.10.13.~2009.11.4. >**

Rev.	Item	Date	Impact	Page	Change Cause	Modify Description
0.7	1	10/13	CKT,BOM,Layout	24	-Change one of the USB Bulk Cap from 150UF to 220UF. <Compal>.	--Change C406 from 150U_B2_6.3VM_R35M (P/N:SGA00002N80) to 220U_6.3V_M (P/N:SF000002Y00).
0.7	2	10/13	CKT,Layout	15,22	-Delete USB20_N6/P6 from WLAN slot. WiMAX is dead. <HP>.	--Delete USB20_N6/P6 between WLAN slot JP6.36/38 and PCH U7.M22/N22.
0.7	3	10/19	CKT,Layout	32	-Delete and modify Skew Hole PCB Footprint for M/E Drawing update. <Compal>.	--Delete H13 (H_3P0); change H2 from H_4P7 to H_4P4; H28 from H_4P9 to H_4P8.
0.7	4	10/19	CKT,BOM,Layout	15,22,31	-Simplify the CLK_PCI_DB and CLK_PCI_DEBUG design and routing for improve EE signals quality and EMI Issue. <Compal>.	--Design change and del R270 to simplify that become CLK_PCI_DEBUG; Add R477 0 ohm to separate for JP6.19 option CLK_PCI_DEBUG connection.
0.7	5	10/21	CKT,Layout	15	-Modify RP1 Pin1,2,3 connection for layout routing smoothly. <Compal>.	--Modify RP1 Pin1,2,3 connection for layout routing smoothly.
0.7	6	11/03	CKT,BOM,Layout	21	-M/E Design change the RJ-45 connector. <Compal>.	--M/E Design change JR145 DC234003O00(TYCO_2006067-T_13P) to DC020910201(FOX_JM36111-R2225-7H_13P-T).
0.7	7	11/03	CKT,BOM,Layout	24	-Add the RC delay circuit between SLP_S4# and SLP_S4_R to fix dual USB can not power on issue. <Compal>.	--Del R697(0_0201); Add R11(470K_0402) and C7(0.01uF) close to U33 pin3 and pin4.
0.7	8	11/05	CKT,BOM,Layout	29	-Add the isolate circuit for Skagen side Monitor Stand HDD LED light on issue fix. <Compal>.	--Design in the isolate circuit on SATA_LED# by add Q79 (2N7002) and R49 (10K) PH close to Docking Connector JP30.39.
0.7	9	11/05	CKT,BOM	29	-Schematic BOM change for actual and common. <Compal>.	--BOM change on Q30, Q19, U6.
0.7	10	11/06	CKT,BOM	30	-Schematic BOM change for CBB Reset function. <HP>.	--BOM change to install R605 (0_0201).
0.7	11	11/06	CKT,BOM,Layout	18	-Add +3VS PH on CRT_DDC_CLK & C_RT_DDC_DATA for design change. <MAXIM>.	--Add R53,R57(2.2K) +3VS pull-high on CRT_DDC_CLK & C_RT_DDC_DATA for MAXIM CRT switch design change.
0.7	12	11/06	CKT,BOM,Layout	4	-Cancel REMOTE thermal sensor reserve. <HP/Compal>.	--Delete REMOTE2+/- traces & Q1. Move C5 close to pins 16/15 of U2.
0.7	13	11/11	CKT,BOM,Layout	14,28	-Add 0.1uF cap for EMI issue fix. <Compal>.	--Add C669 (0.1uF) close to R215; C668 (0.1uF) close to JP22.2.
0.7	14	11/11	CKT,BOM	20	-Install EMI INV_PWM reserve solution for issue fix. <Compal>.	--Install R372 (22_0402) and C665 (220P_0402).
0.7	15	11/11	CKT,BOM,Layout	28	-Add 0.1uF CAP on ON/OFF# for ESD issue fix. <Compal>.	--Add C670 (0.1uF_0402) close to JP20.2's via.
0.7	16	11/12	CKT,BOM,Layout	28	-Add 0 ohm resistor for CBB reset function pin ground to avoid floating. <SMsC/Compal>.	--Add R60 (0_0402) close JP28 pin 3 for CBB reset function reserve.
0.7	17	11/12	CKT,BOM,Layout	38	-To resolve glitch seen on +0.75VS power rail during S0->G3 transition. <HP/Compal>.	--Add power jumper options for +1.5VS_CPU_VDDQ(PJP605) & +1.5V(PJP604) to PU601.1. Make PJP605 option installed.
0.7	18	11/12	CKT,Layout	29	-To resolve Docking Connector (JP30) SMT soldering issue. <HP/Compal>.	--Update the symbol and PCB Footprint FOX_QL1044L-D261A1-7H_82P-T for fix.
0.7	19	11/12	CKT,BOM	-	-Schematic BOM change for actual and common. <Compal>.	--BOM change on C68,C69,C70,C71,C72,C92,C93,C94,C113,C114,C115,C140_C63,C64,C65,C66,C67,C85,C86,C87,C88,C89,C90,C91; C29,C60,C48,C62; C30;
0.7	20	11/13	CKT,BOM,Layout	32	-M/E Screw hole size modify. <Compal/HP>.	--Change H2 from H_4P4 to H_4P7; H28 from H_4P8 to H_4P9.
0.7	21	11/13	CKT,BOM	25	-To fix CBB auto active caused by +3VS leakage issue. <Compal>.	--Change Q28 from AP2301(SB000007H10) to AP2309(SB00000MI00).
0.7	22	11/13	CKT,BOM	13	-To follow INTEL Design Guide Requirement. <INTEL>.	--Change C193,C194,C195,C196,C197,C198 from 0.1U_0402_16V4Z(SE070104Z80) to 0.1U_0402_25V4K(SE00000G880).
0.7	23	11/14	CKT,BOM,Layout	28,30	-Cancel CAP_RST related design reserve to avoid the ESD issue. <HP/SMsC>.	--Del CAP_RST Net and also R60,R605, leave the KBC pin63 (GPIO35) alone as NC.
0.7	24	11/27	CKT,BOM	14,18	-BOM change for CRT EMI and EE SVTP fail issue. <HP/Compal>.	--Remove R247,R248,R249 (150_0402); Install C232,C233,C234 (18P_0402); Remove C235,C236,C237 (18P_0402); Change L2,L4,L6 from 0805CS-111XJLC_0805 to 0_0603_5%; Change L1,L3,L5 from 0805CS-111XJLC_0805 to HLC0603CSCC33NJT_0603; Remove R322,R323,R324 (150_0402_1%); Install C321,C320,C315 (75_0402_1%)
0.7	25	11/27	CKT,BOM	7	-To fix INTEL Leakage circuit sequence issue. <HP/Compal>.	--Change C26,C27 from 10uF(SE093106M80) to 22uF(SE000000I10); also change the soldering pad from PJP604 to PJP605.

**KAT10 from PV-R to Pre-MV LA-5251P REV:0.8 -> 0.9 Modify <2009.12.29.~2010.01.05. >**

Rev.	Item	Date	Impact	Page	Change Cause	Modify Description
0.9	1	01/04	CKT,BOM,Layout	30,31	-Need rotate the BIOS Socket for new type one implement without repair and SMT interfere issue. <Compal>.	--1. Cancel 16pin BIOS reserve (Del U36 and R696); 2. Cancel Board ID Detect reserve circuit (Del U8,Q37,R571,R572,R574,R575);
0.9	2	01/04	Layout	29	-To final Foxconn Docking Connector layout footprint. <Compal>.	3. Rotate 8 pin BIOS Socket 90 degree.
0.9	3	01/04	CKT,Layout	32	-Cancel H17 Screw Hole for M/E design change. <Compal>.	--Update PCB Footprint (FOX_QL1044L-D261A1-7H_82P-T) from Compal Server -> No change and same as PV phase.
0.9	4	01/04	CKT,BOM,Layout	4,14,28	-Add Caps for ESD CBB issue fixed. <Compal>.	--Cancel H17 Screw Hole for M/E design change.
0.9	5	01/04	CKT,BOM,Layout	14	-Reduce L1~L6 package size for fix repair and SMT issue. <Compal>.	--Add C119 between JP4 pin 37 and 41; Add C120 close to R20.1; Add C145 close to R231 pin 1; Add C146 close to D34 pin 1.
0.9	6	01/05	CKT,BOM,Layout	33	-Add Cut Mode Caps for EMI PCI issue fix. <Compal>.	--1. Change L2,L4,L6 PCB Footprint from TAIYO_LB2012T100MR_L2012_2P to R_0603 for final. 2. Change L1,L3,L5 from TAIYO_LB2012T100MR_L2012_2P to KC_HLC0603CSCC33NJT_2P for final. --Add 4 pcs 0.1uF Cut Mode Caps (C666,C667,C671) which located around the canceled Braidwood module. for EMI PCI issue fix.

Security Classification		Compal Secret Data		Title	
Issued Date	2006/02/13	Deciphered Date	2010/12/31	H/W2 EE Dept. PIR SHEET(2)	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. THIS SHEET MAY NOT BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, WITHOUT THE WRITTEN PERMISSION OF COMPAL ELECTRONICS, INC.				Size	Rev
				Customer	0.9
				Date	Tuesday, January 05, 2010
				Sheet	47 of 47